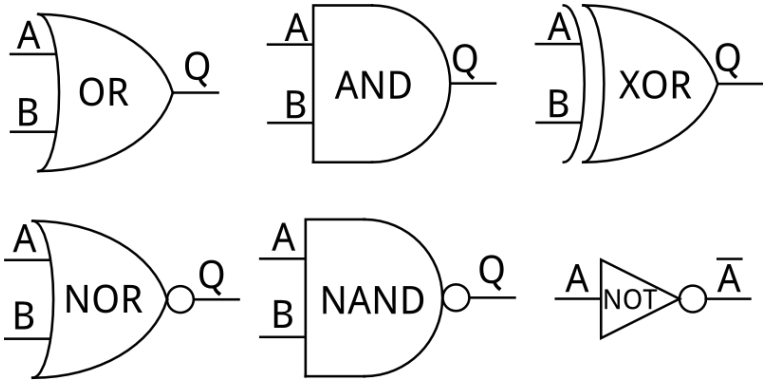
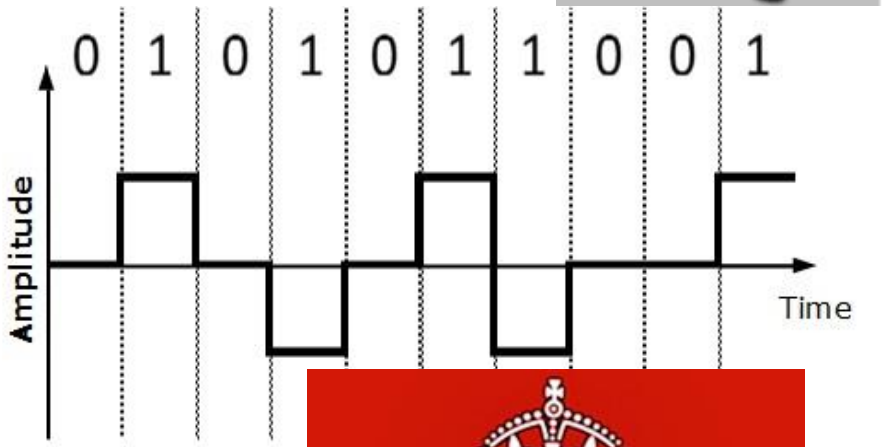
# Proiectare Logica

## Digital Logic Design

# Lab 11

cnic.ro





# Proiectati un NR sincron

- **Pe 3 biti care sa numere conform secventei :**

  **1→3→5→7→1; 2→1; 4→3; 6→ 5; 0→1**

  **atat cu BB de tip D cat si cu BB de tip JK**
- **Verificati functionarea corecta a lor in wronex**

**JK Excitation table**

| Q | $Q_{next}$ | J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

# Numaratoare sicrone cu BB tip D si cu BB de tip JK

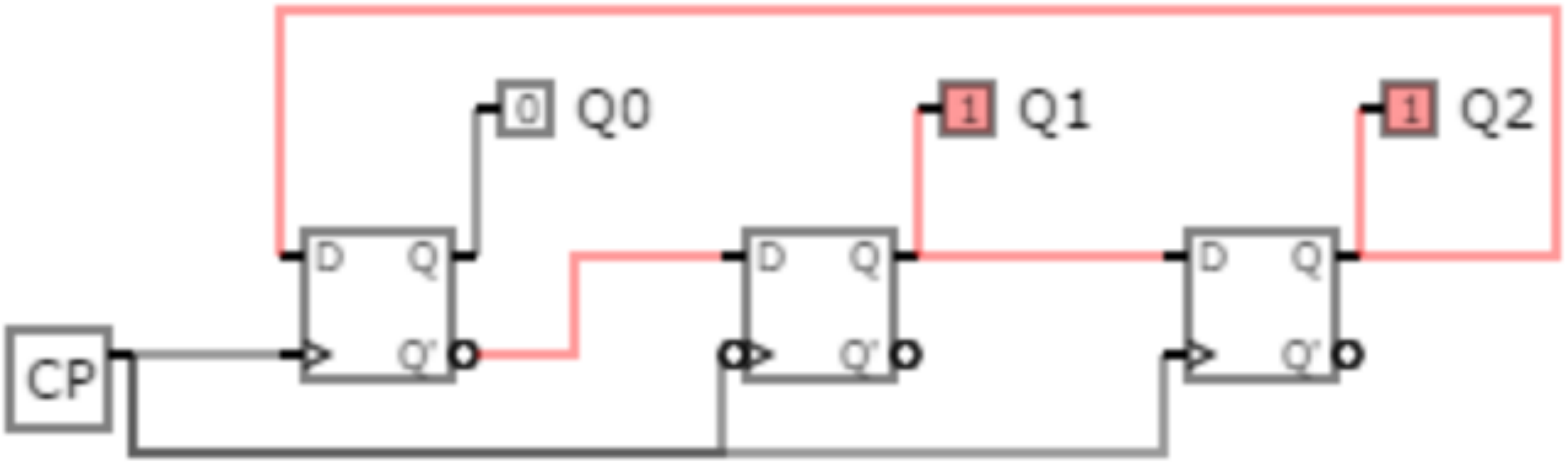
Proiectati si verificati in wronex numaratoarele ce functioneaza conform diagramelor de stari:

1. 5-2-0-4-5; 6-1-7-3-0;
2. 5-7-2-5; 3-6-4-0-1-6;
3. 6-0-2-1-4-6; 7-5-0; 3-1;
4. 1-3-5-7-1; 0-1; 2-3; 4-5; 6-7;
5. 12-5-3-9-13-2-10-8-7-12; 15-14-6-5; 4-11-1-0-2;

| Q | $Q_{next}$ | J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

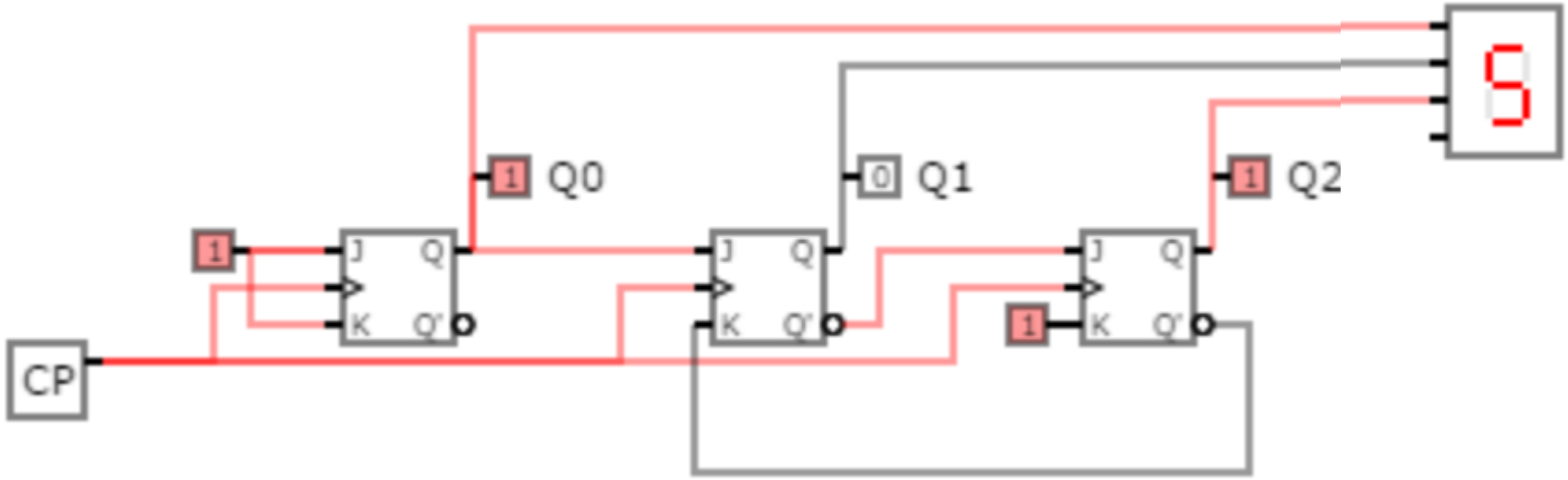
# Problema 2

- Implemetati in wronex schema de mai jos folosind varianta de BB cu S si R.
- Folosind aceasta pagina desenati formele de unda pentru semnalele CLOCK, Q0, Q1 si Q2.
- Desenati graful starilor acestui numarator.



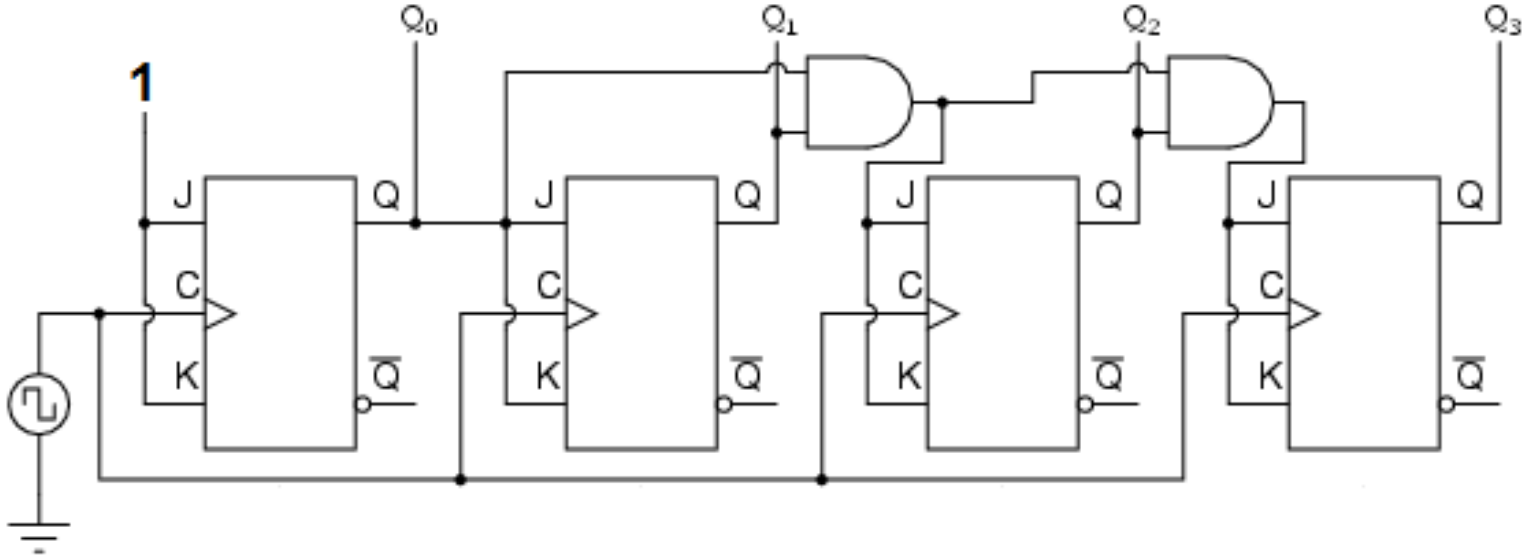
# Problema 3

- Implemetati in wronex schema de mai jos folosind varianta de BB cu S si R.
- Folosind aceasta pagina desenati formele de unda pentru semnalele CLOCK, Q0, Q1 si Q2.
- Desenati graful starilor acestui numarator.

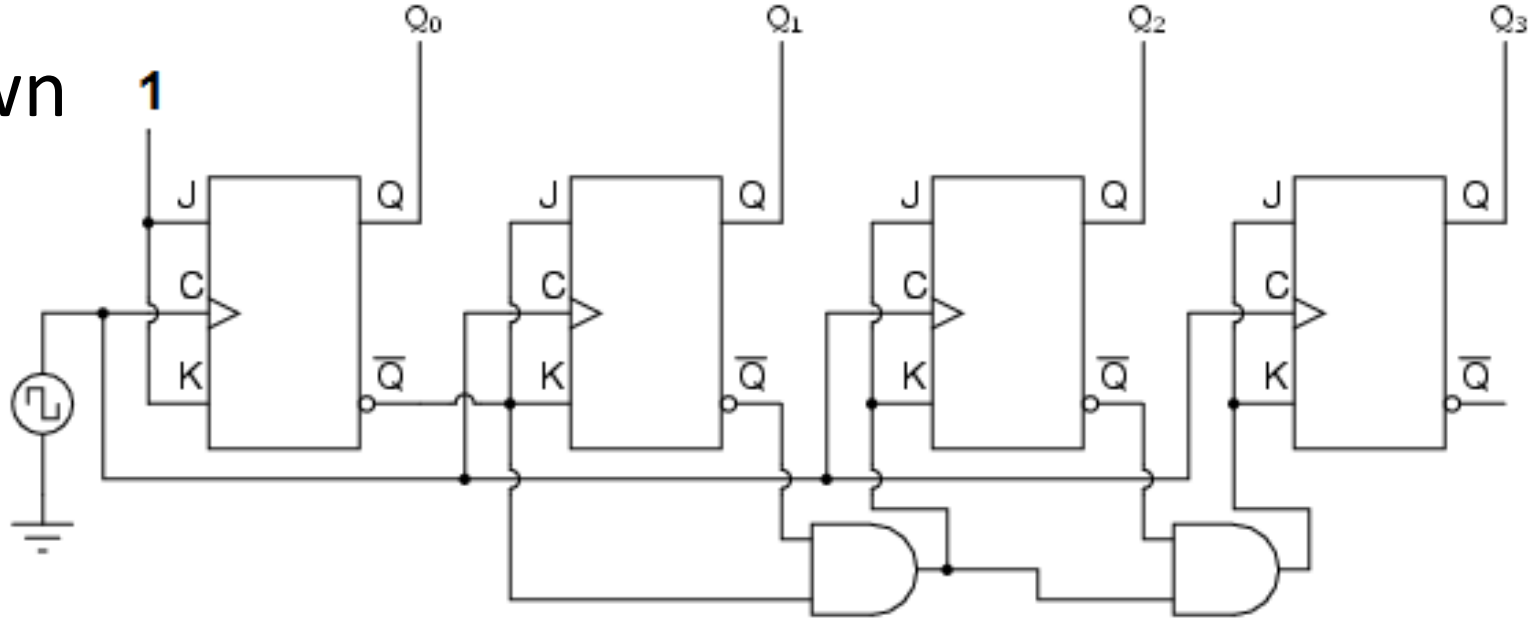


# Numaratoare sincrone Up sau Down

- NR Up

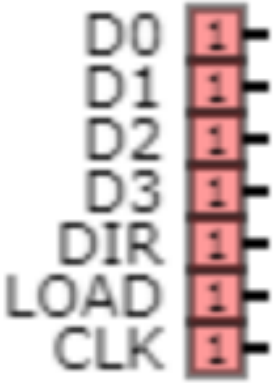


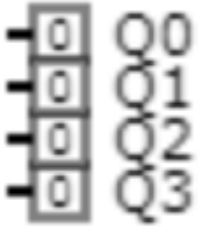

- NR Down

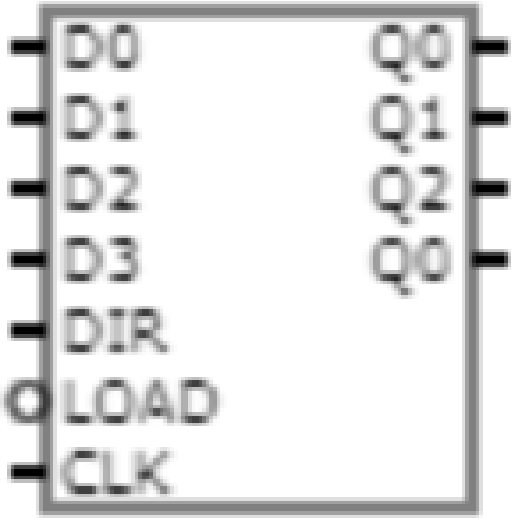


# Problema 4

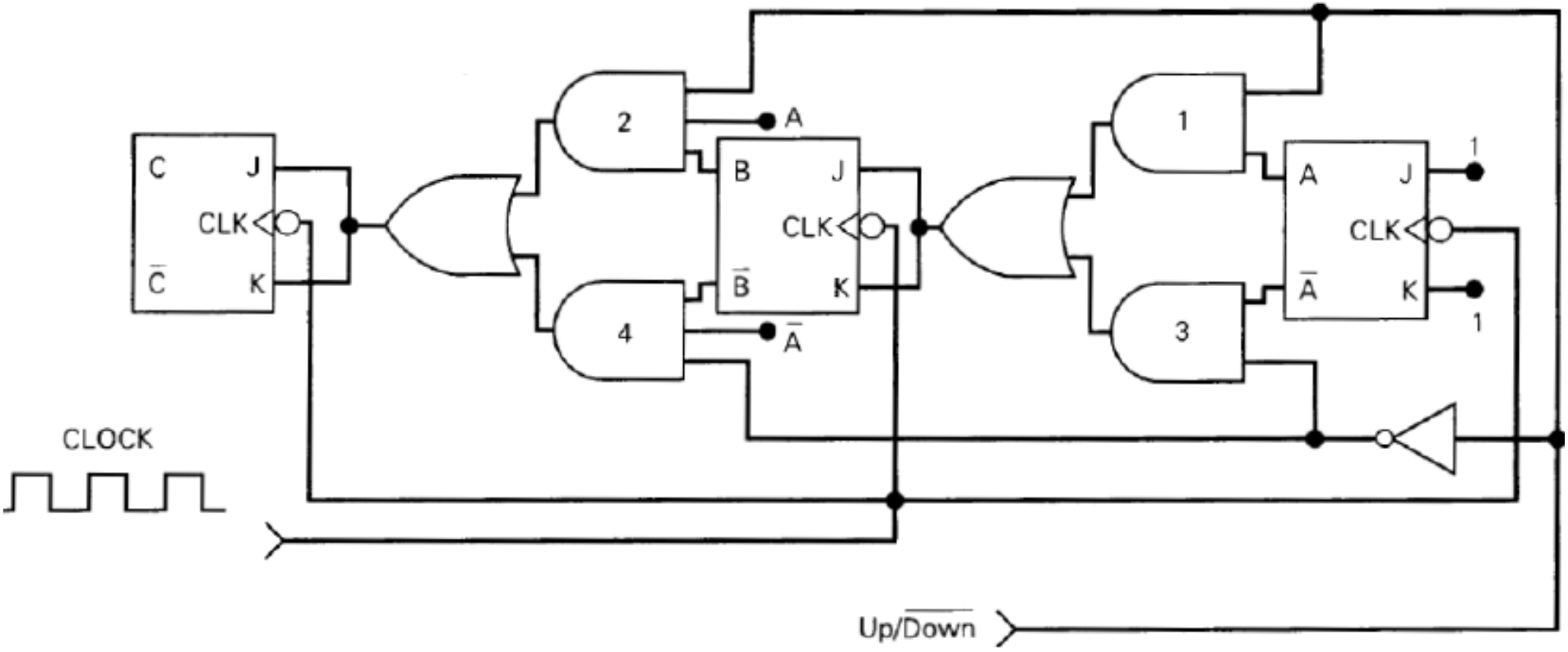
Implementati un NR sincron, pe 4 biti, bidirectional (poate numara Up/Down, in functie de starea unei intrari DIR), cu intrare de LOAD asincrona, activa in starea L! Folositi BB JK+SR! Daca intrarea DIR=0/1 →Down/Up. **Indicatie:** implementati un NR up (iesirile qx). Folositi **Qx=DIR⊕qx** pentru DIR; **Sx=LOAD.Dx** si **Rx=LOAD.Dx'** pentru preincarcarea bistabililor!



# Pb 5. Ce face acest circuit?



# Problema 6 – '193

Sa se implementeze acest gate