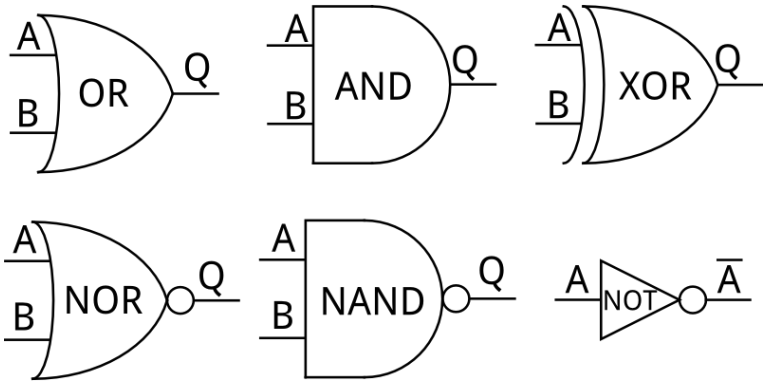
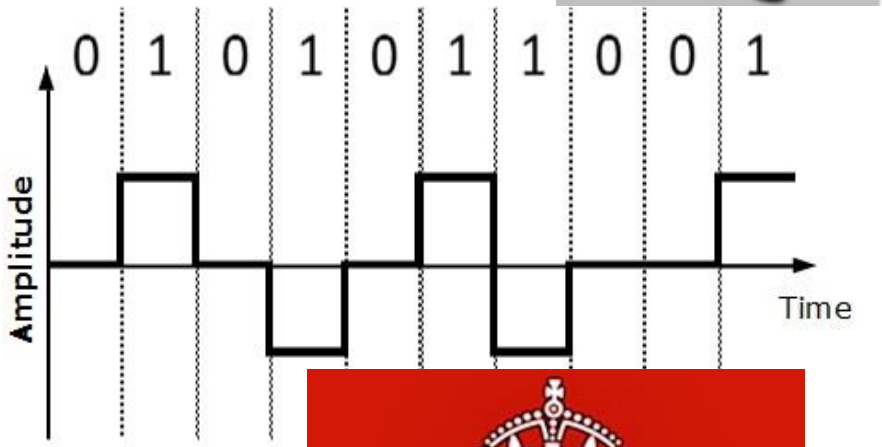
Proiectare Logica

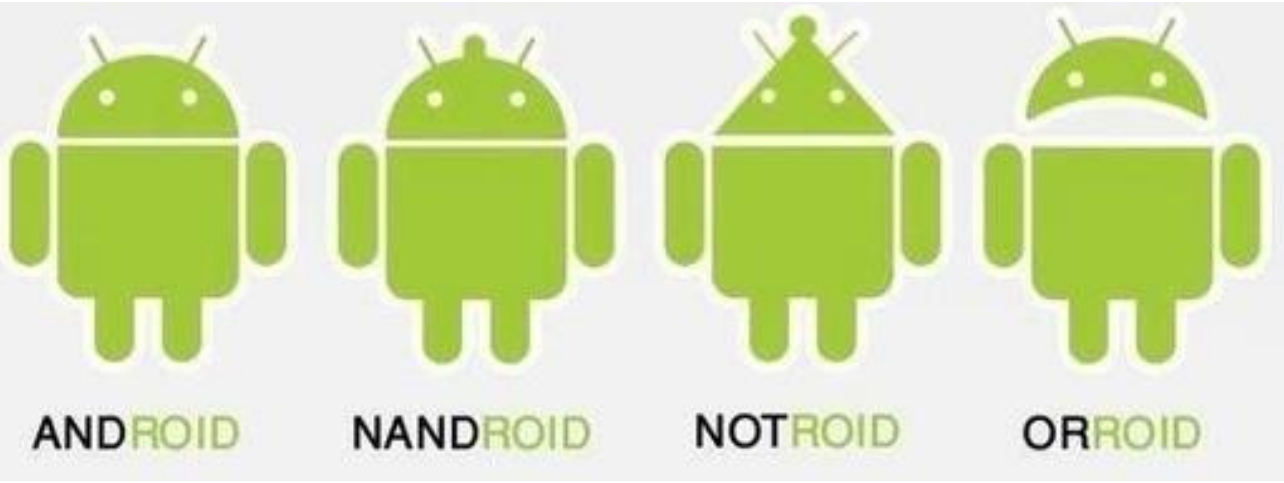
Digital Logic Design

Lab 09

cnic.ro



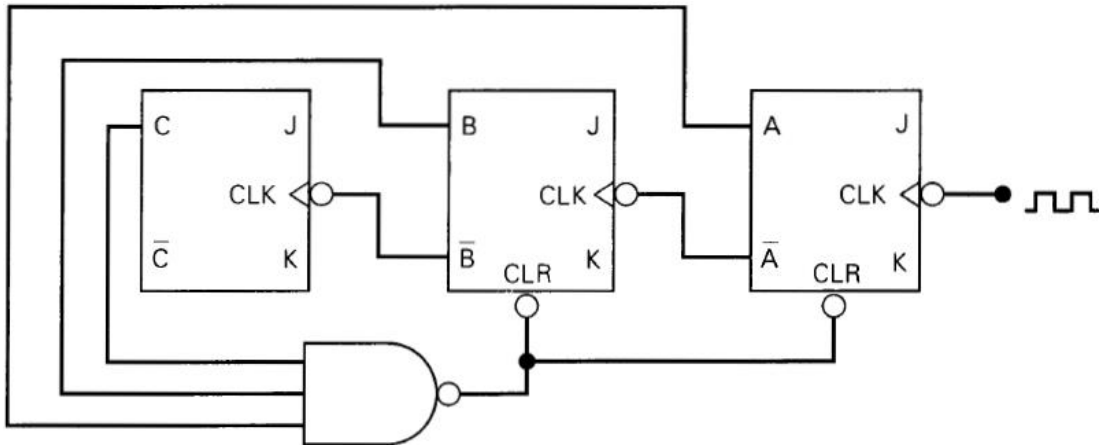




Studiu

TEMA: Simulati in Wronex folosind linii de intarziere pentru semnalele de clock dintre bistabile numaratorul din schema alaturata! Toate JK-urile sunt in 1.

- Identificati ordinea de numarare!



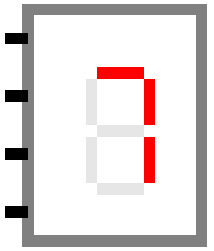
Simulati in wronex urmatoarele circuite

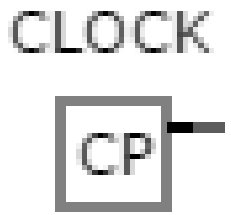
Lucrul cu numaratoarele:

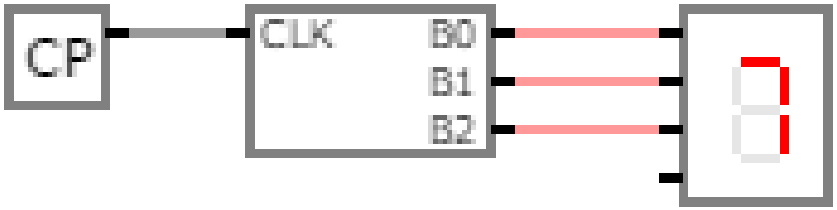
Folositi Afisorul cu 7 segmente si

Generatorul de CLOCK

si incapsulati schemele pentru a putea fi folosite cu Add as gate

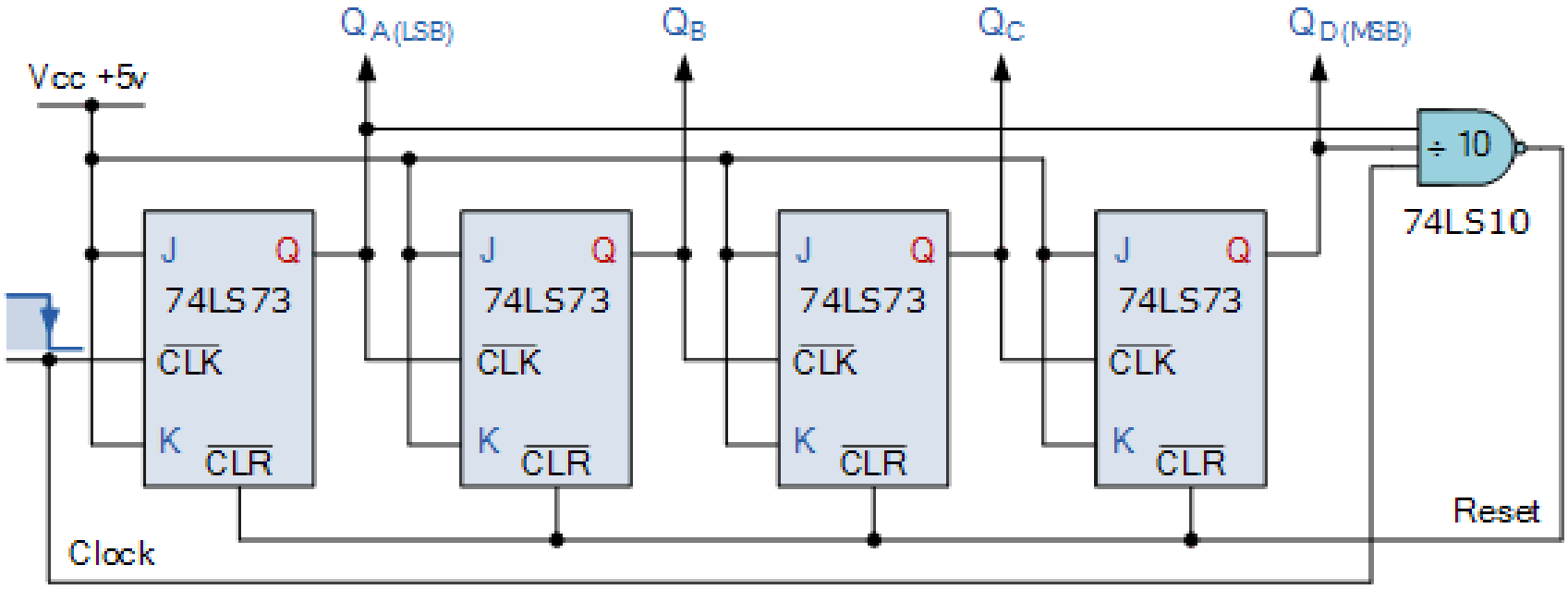






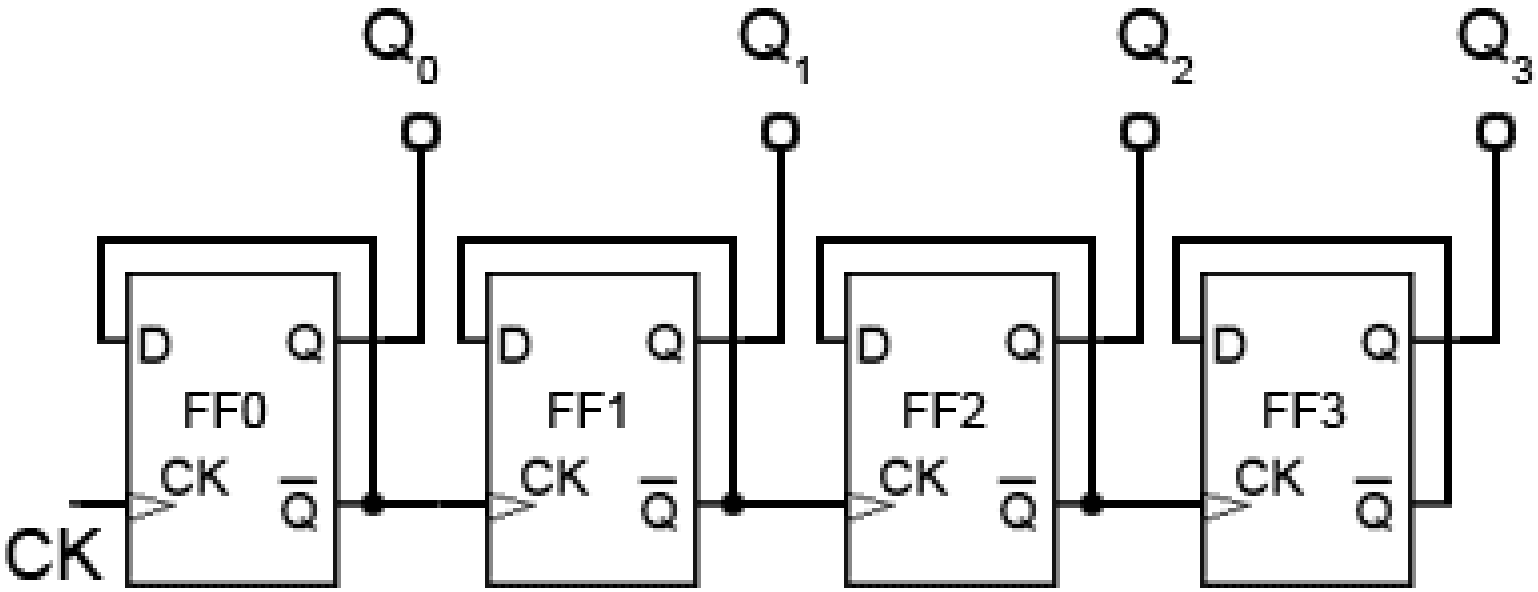
1

- Cu BB de tip JK



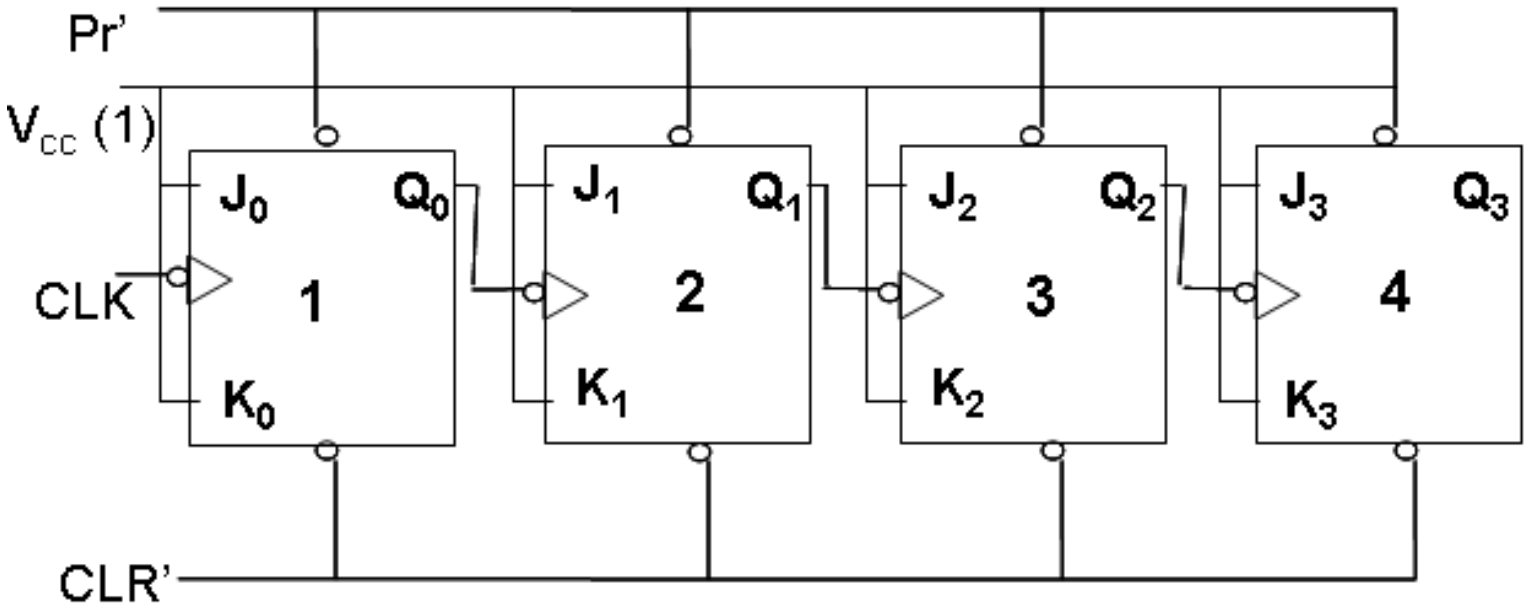
2

- Cu BB de tip D



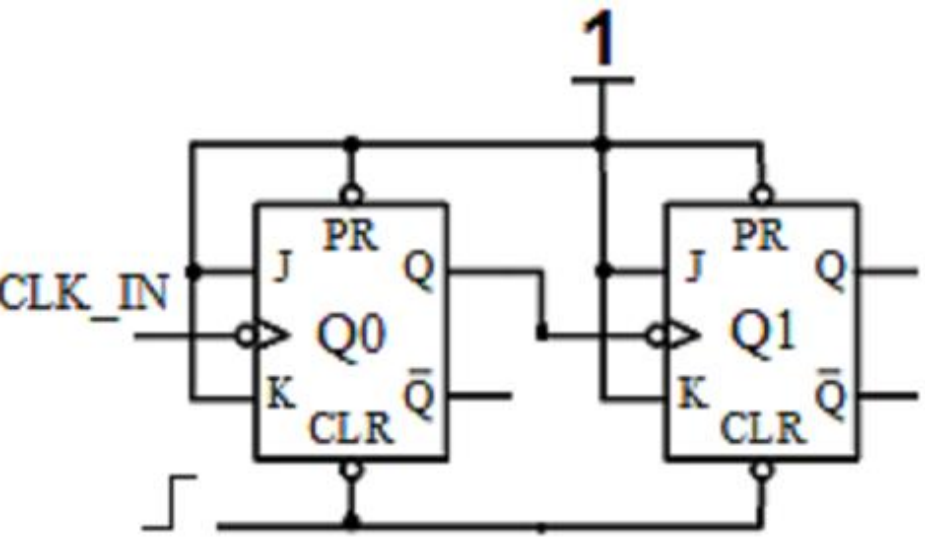
3

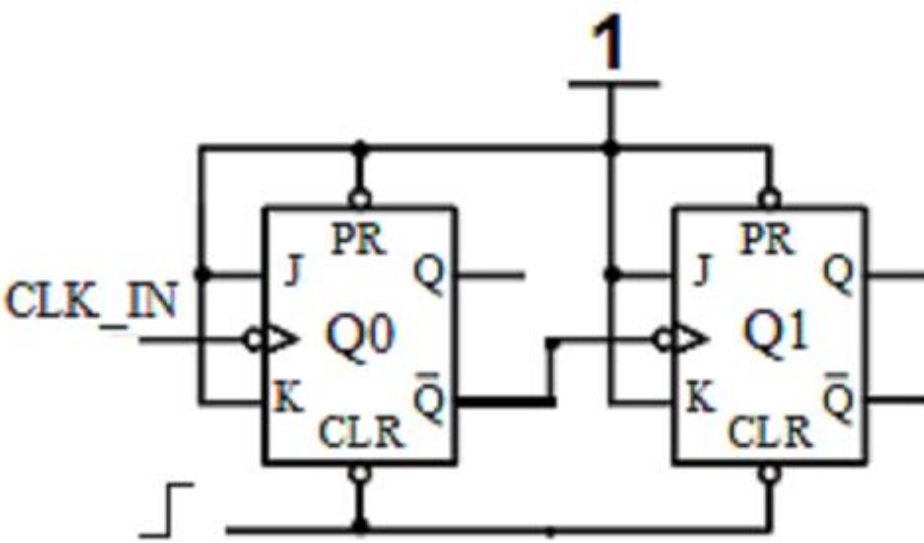
- Cu BB de tip JK



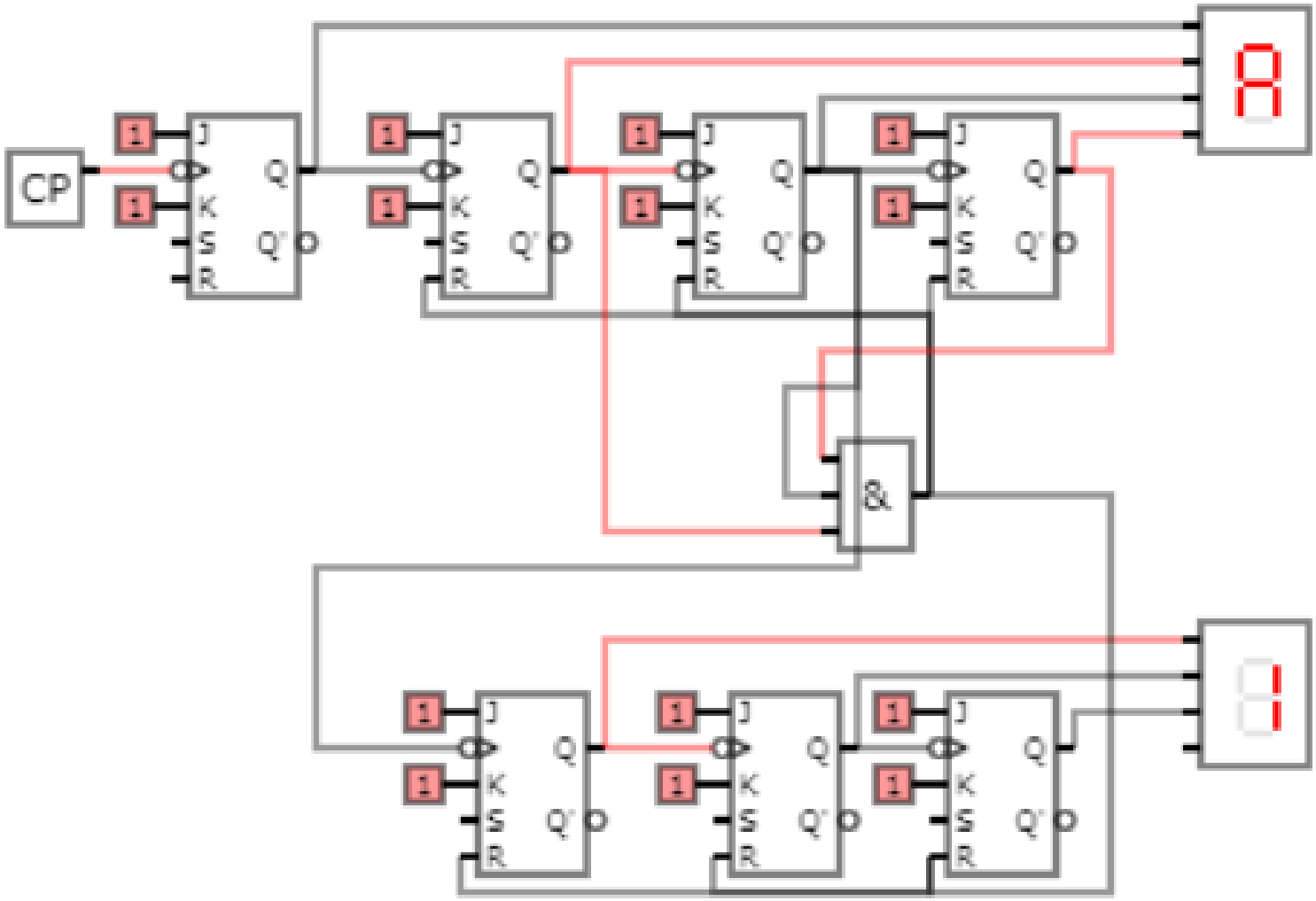
4

- Cu BB de tip JK





Implementati in wronex!

- 

Diagrame V-K

ce contin stari NU CONTEAZA

Tabela de adevar

A	B	F (AB)
0	0	X
0	1	0
1	0	X
1	1	1

Sa se minimizeze

- Fie functiile:

A	B	C	F(ABC)
0	0	0	0
0	0	1	X
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	X
1	1	0	X
1	1	1	0

A	B	C	F(ABC)
0	0	0	0
0	0	1	X
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	X
1	1	0	X
1	1	1	1

Sa se minimizeze

- Fie functiile:

A	B	C	F (ABC)
0	0	0	0
0	0	1	X
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	X
1	1	1	X

A	B	C	F (ABC)
0	0	0	1
0	0	1	X
0	1	0	0
0	1	1	X
1	0	0	X
1	0	1	1
1	1	0	0
1	1	1	X

Sa se minimizeze

- Fie functiile:

A	B	C	F (ABC)
0	0	0	X
0	0	1	X
0	1	0	1
0	1	1	0
1	0	0	X
1	0	1	1
1	1	0	X
1	1	1	X

A	B	C	F (ABC)
0	0	0	1
0	0	1	X
0	1	0	0
0	1	1	1
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	1

Sa se minimizeze

- Fie functiile:

A	B	C	D	F(ABCD)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	X
0	1	0	1	X
0	1	1	0	X
0	1	1	1	0
1	0	0	0	0
1	0	0	1	X
1	0	1	0	0
1	0	1	1	0
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	1

A	B	C	D	F(ABCD)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	X
0	0	1	1	0
0	1	0	0	X
0	1	0	1	X
0	1	1	0	X
0	1	1	1	0
1	0	0	0	1
1	0	0	1	X
1	0	1	0	X
1	0	1	1	1
1	1	0	0	X
1	1	0	1	X
1	1	1	0	1
1	1	1	1	X

Sa se minimizeze

- Fie functiile:

A	B	C	D	F(ABCD)
0	0	0	0	1
0	0	0	1	X
0	0	1	0	X
0	0	1	1	0
0	1	0	0	X
0	1	0	1	X
0	1	1	0	X
0	1	1	1	1
1	0	0	0	X
1	0	0	1	0
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	1
1	1	1	1	X

A	B	C	D	F(ABCD)
0	0	0	0	0
0	0	0	1	X
0	0	1	0	X
0	0	1	1	0
0	1	0	0	X
0	1	0	1	X
0	1	1	0	X
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	1
1	1	1	1	X

Sa se minimizeze

- Fie functiile:

	00	01	11	10
00	1	x	x	1
01	x	1	x	1
11	x	1	0	0
10	x	0	x	1

Problema ca la examen NR asincron

- Fie un sistem de 4 BB de tip JK adusi in regim de toggle, numerotati de la 0-3, ale caror intrari de CK au polaritatile: +-+-. Sistemul devine un numarator daca facem urmatoarele conexiuni: CK0=Q1; CK1=Q3; CK2=CLOCK; CK3=!Q2.
- Desenati schema electronica a acestui numarator.
- Simulati in wronex aceasta schema. Folositi BB JK cu S si R.
- Desenati formele de unda (**folosind aceasta pagina)** pentru semnalele CLOCK, Q0, Q1, Q2 si Q3 pentru 17 perioade ale semnalului de ceas, incepand cu starea 4 pe semiperioada cand semnalul de clock este L.

Problema ca la examen NR sincron

Fie 3 BB de tip JK, numerotati de la 0-2, avand polaritatile semnalelor CK -+-. Acest sistem devine un numarator daca semnalul CLOCK este legat la toate semnalele CK ale bistabilelor si sunt facute urmatoarele conexiuni: J0=1; K0=!Q1; J1=Q2; K1=Q0; J2=Q0 si K2=!Q1.

1. Desenati schema electronica a acestui numarator.

2. Desenati formele de unda pe caiet pentru semnalele CLOCK, Q0, Q1 si Q2 pentru 6 perioade ale semnalului de clock, incepand cu starea 2 pe semiperioada cand semnalul de clock este L. (6p)

- Simulati in wronex aceasta schema. Folositi BB JK cu S si R.
- Desenati formele de unda (**folosind aceasta pagina)** pentru semnalele CLOCK, Q0, Q1, Q2.

Problema ca la examen

Fie 3 BB de tip JK, numerotati de la 0-2, avand polaritatile semnalelor CK -++. Acest sistem devine un numarator daca semnalul CLOCK este legat la toate semnalele CK ale bistabilelor si sunt facute urmatoarele conexiuni: J0=1; K0=!Q1; J1=Q2; K1=Q0; J2=Q0 si K2=!Q1.

1. Desenati schema electronica a acestui numarator.

2. Desenati formele de unda pe caiet pentru semnalele CLOCK, Q0, Q1 si Q2 pentru 6 perioade ale semnalului de clock, incepand cu starea 6 pe semiperioada cand semnalul de clock este H. (6p)

- Simulati in wronex aceasta schema. Folositi BB JK cu S si R.
- Desenati formele de unda (**folosind aceasta pagina)** pentru semnalele CLOCK, Q0, Q1, Q2.