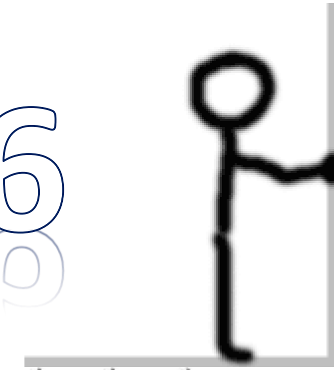
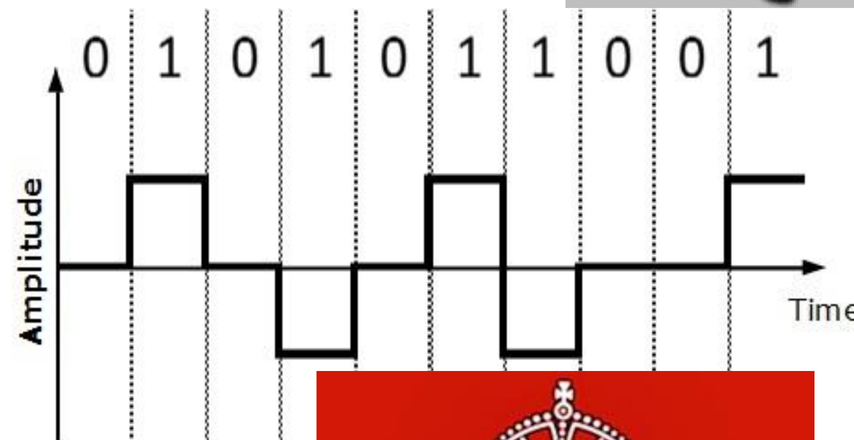
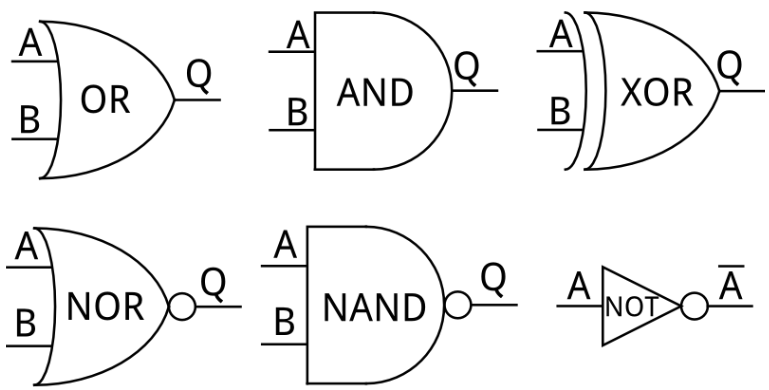
Proiectare Logica

Digital Logic Design

Curs 06







Exemplu de subiect la Partial

1. Scrieti numarul 757_8 in baza 10. (1p)

2. Care sunt primele 5 cifre dupa virgula ale numarului 0.57910 in baza 8. (1p)

3. Scrieti tabela de adevar a functiei F(ABCD)=A.B'+B.C'.D'+B'.D+A'.C . Gasiti mintermenii acestei functii şi scrieţi FCD. (2p)

4. Functia f cu patru variabile are maxtermenii (11,13,9,8,6,15,5,3,1,7,10,4). Minimizati aceasta functie folosind diagramele Veitch. (3p)

5. Gasiti reprezentarea in binary64 a numarului -7.3437510 (bit semn, exponent si mantisa) (2p)

Diagrame Karnaugh 3 variabile

- Diagramele Karnaugh (K maps) continua in mod logic diagramele Veitch

Tabela de adevar

A	B	C	F (ABC)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Diagrama Karnaugh

		AB			
		00	01	11	10
C	0	0	1	1	0
	1	1	0	0	1

Diagrama Veitch

			A	A
	0	1	1	0
C	1	0	0	1
		B	B	

Diagrame Karnaugh 4 variabile

- Diagramele Karnaugh (K maps) continua in mod logic diagramele Veitch

Tabela de adevar

A	B	C	D	F (ABCD)
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Diagrama Karnaugh

		AB			
		00	01	11	10
CD	00	1	0	0	1
	01	0	1	1	0
	11	0	1	1	0
	10	1	0	0	1

Diagrama Veitch

A

1	0	0	1
0	1	1	0
0	1	1	0
1	0	0	1

D

C

B

Diagrame V-K

- 1. Functia f cu patru variabile are mintermenii (15,2,5,13,11,6,14,10,8,3,7,1). Minimizati aceasta functie folosind diagramele Veitch.

$$sol[0]=A\cdot\overline{B}\cdot\overline{D} + \overline{A}\cdot D + C + B\cdot D$$

- 2. Functia f cu patru variabile are maxtermenii (3,13,14,12,5,11,8,0,2,10,7,6). Minimizati aceasta functie folosind diagramele Veitch. {m(1,4,9,15)}

$$sol[0]=\overline{A}\cdot B\cdot\overline{C}\cdot\overline{D} + \overline{B}\cdot\overline{C}\cdot D + A\cdot B\cdot C\cdot D$$

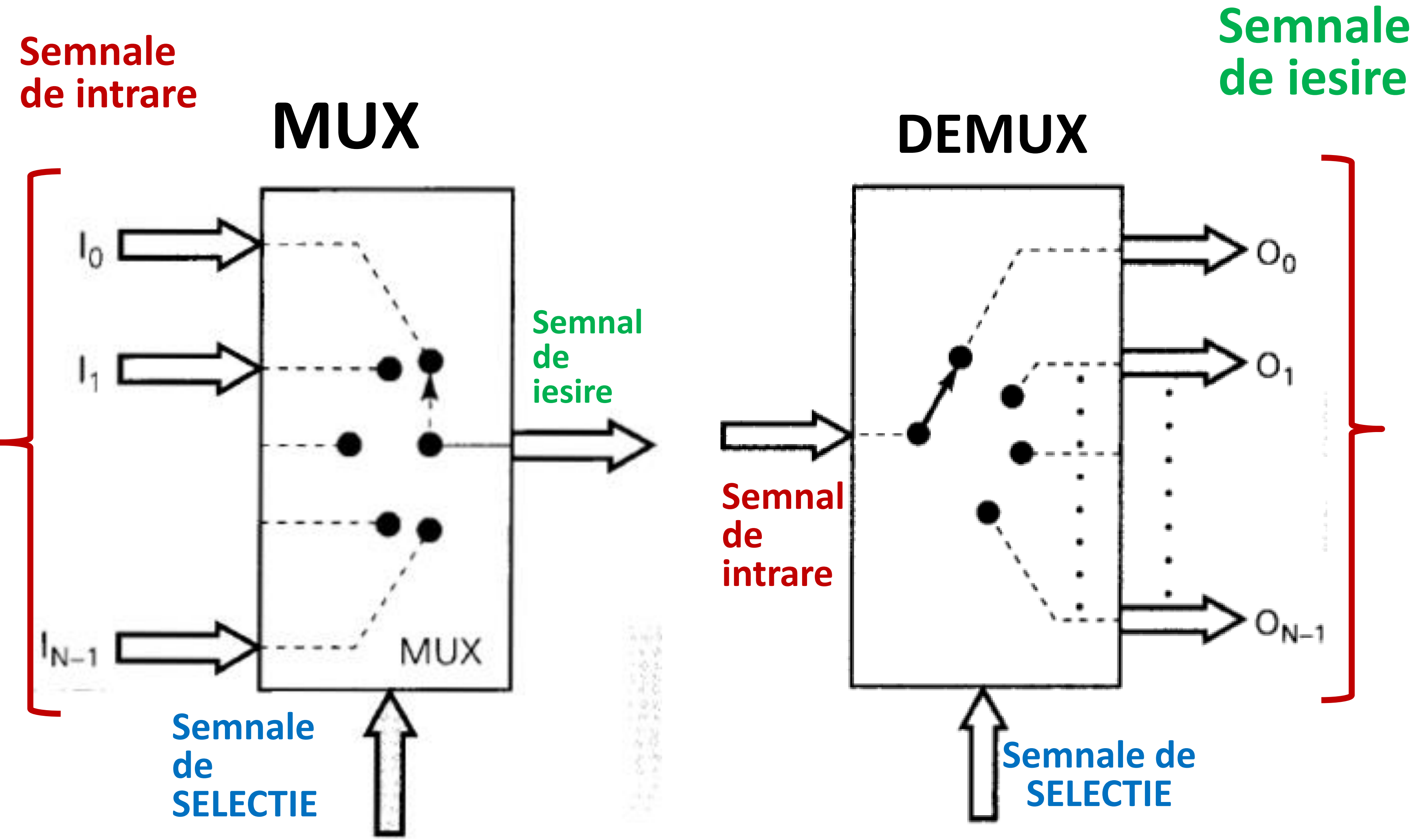
Diagrame V-K

- 3. Functia f cu patru variabile are mintermenii (10,0,5,15,6,1,9,7,14,11,8,13). Minimizati aceasta functie folosind diagramele Veitch.

$$sol[0]=\overline{B}\cdot\overline{C} + B\cdot C + B\cdot D + A\cdot C$$
$$sol[1]=\overline{B}\cdot\overline{C} + B\cdot C + A\cdot\overline{B} + B\cdot D$$
$$sol[2]=\overline{B}\cdot\overline{C} + B\cdot C + \overline{C}\cdot D + A\cdot C$$
$$sol[3]=\overline{B}\cdot\overline{C} + B\cdot C + \overline{C}\cdot D + A\cdot\overline{B}$$

- 4. Functia f cu patru variabile are maxtermenii (0,5,15,6,1,9,7,14,10,11,8,13). Minimizati aceasta functie folosind diagramele Veitch. {m(2,3,4,12)}

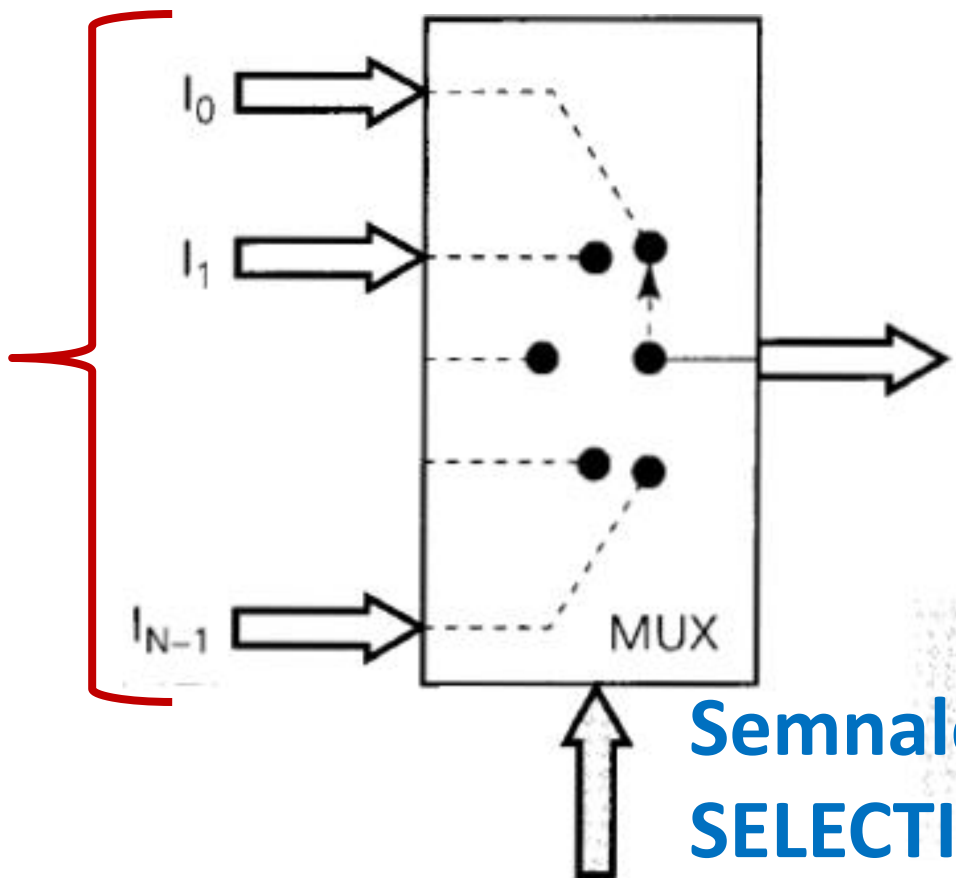
MUX - DEMUX


Semnale de intrare
MUX
I_0
I_1
I_{N-1}
MUX
Semnal de iesire
Semnale de SELECTIE
DEMUX
Semnale de iesire
Semnal de intrare
O_0
O_1
O_{N-1}
Semnale de SELECTIE

Multiplexers (MUX - *Data Selectors*)

- Circuitul are mai multe intrari digitale.
- Numai una dintre intrari este SELECTATA pentru a fi transmisa la iesire.

Semnale de intrare



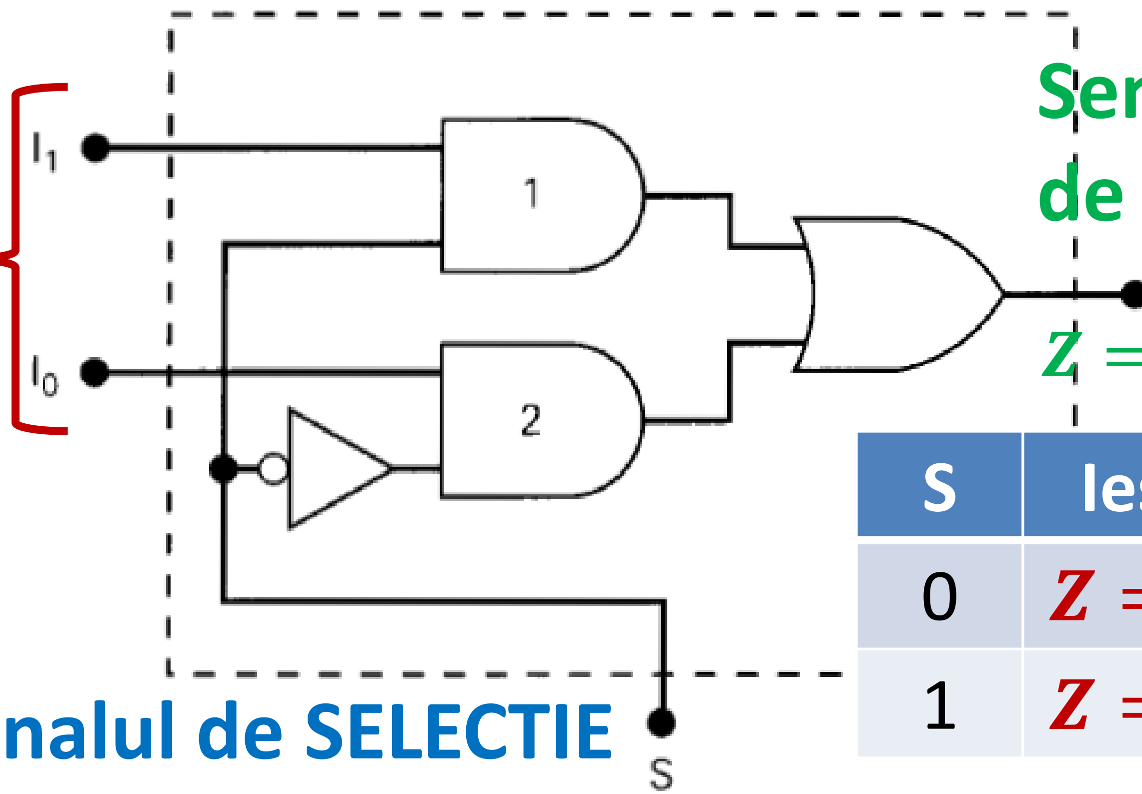
Semnalul de iesire

Semnale de SELECTIE

MUX cu doua intrari

- Circuitul are 2 intrari digitale.
- Formula de functionare este: $Z = I_0\bar{S} + I_1 S$

Semnale de intrare



Semnalul de iesire

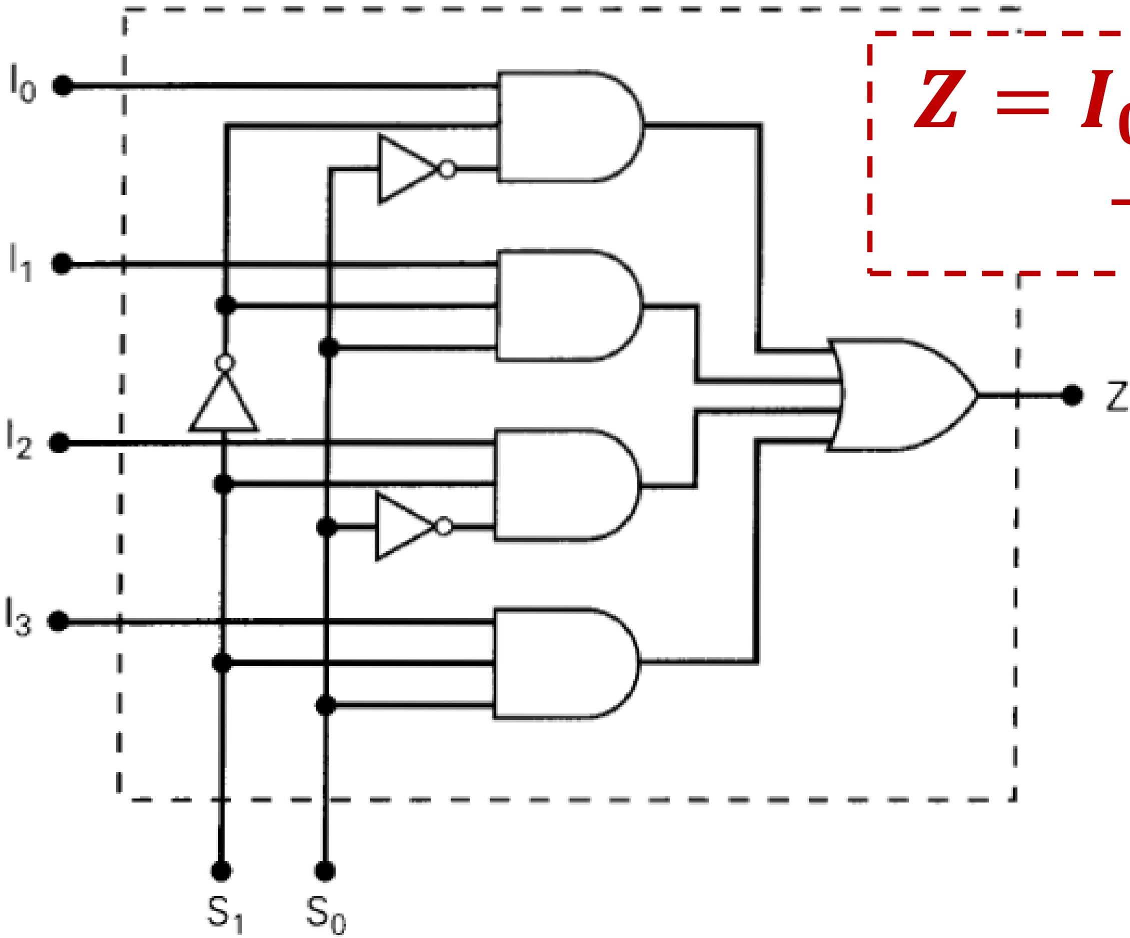
$Z = I_0\bar{S} + I_1 S$

Semnalul de SELECTIE

S	Iesire
0	$Z = I_0$
1	$Z = I_1$

MUX cu patru intrari

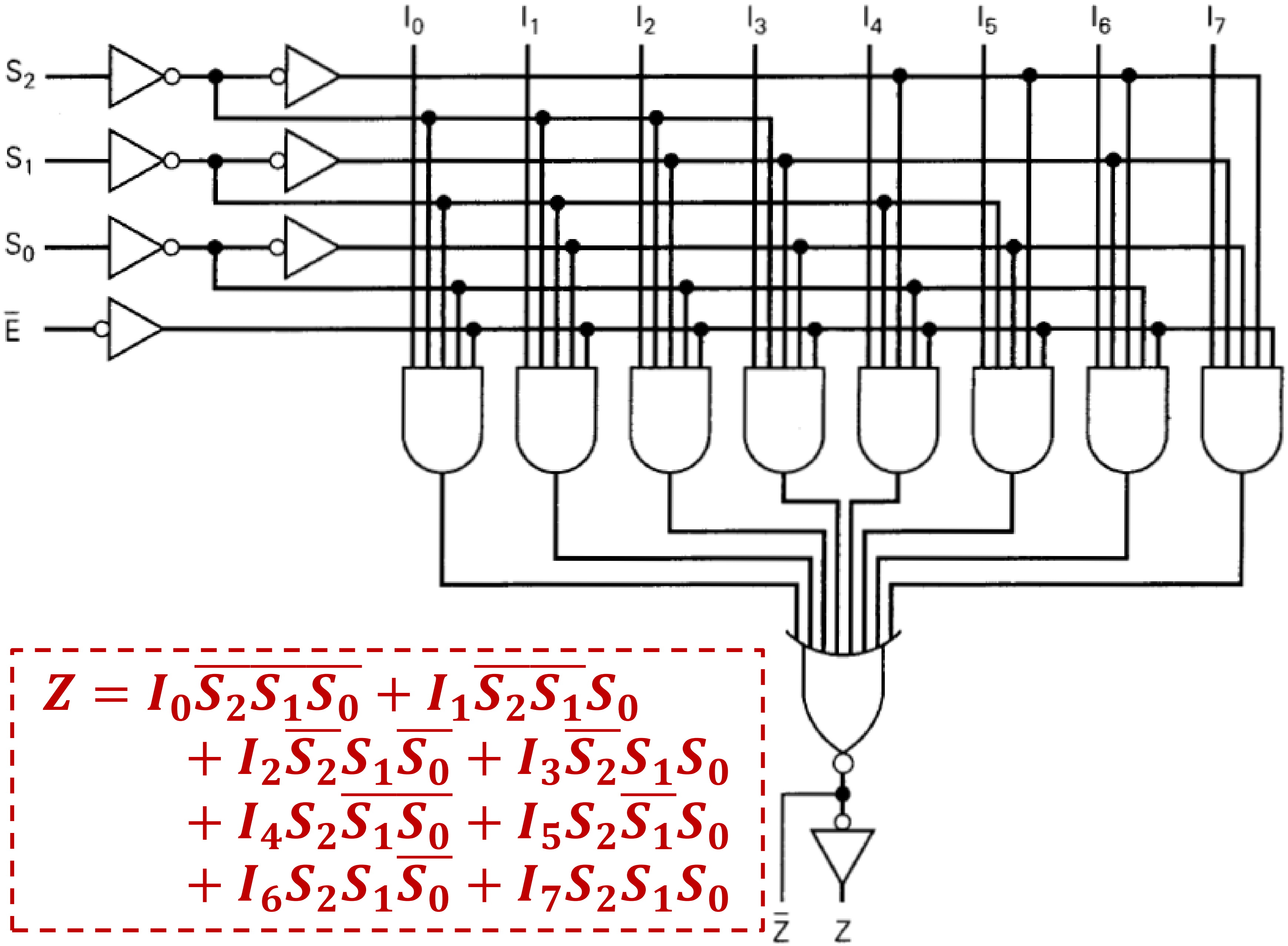
- Circuitul are 4 intrari digitale.
- Formula de functionare este:



$$Z = I_0\overline{S_0}\,\overline{S_1} + I_1\overline{S_0}S_1 + I_2S_0\overline{S_1} + I_3S_0S_1$$

S_0	S_1	Iesire
0	0	$Z = I_0$
0	1	$Z = I_1$
1	0	$Z = I_2$
1	1	$Z = I_3$

MUX cu opt intrari – ex teoretic

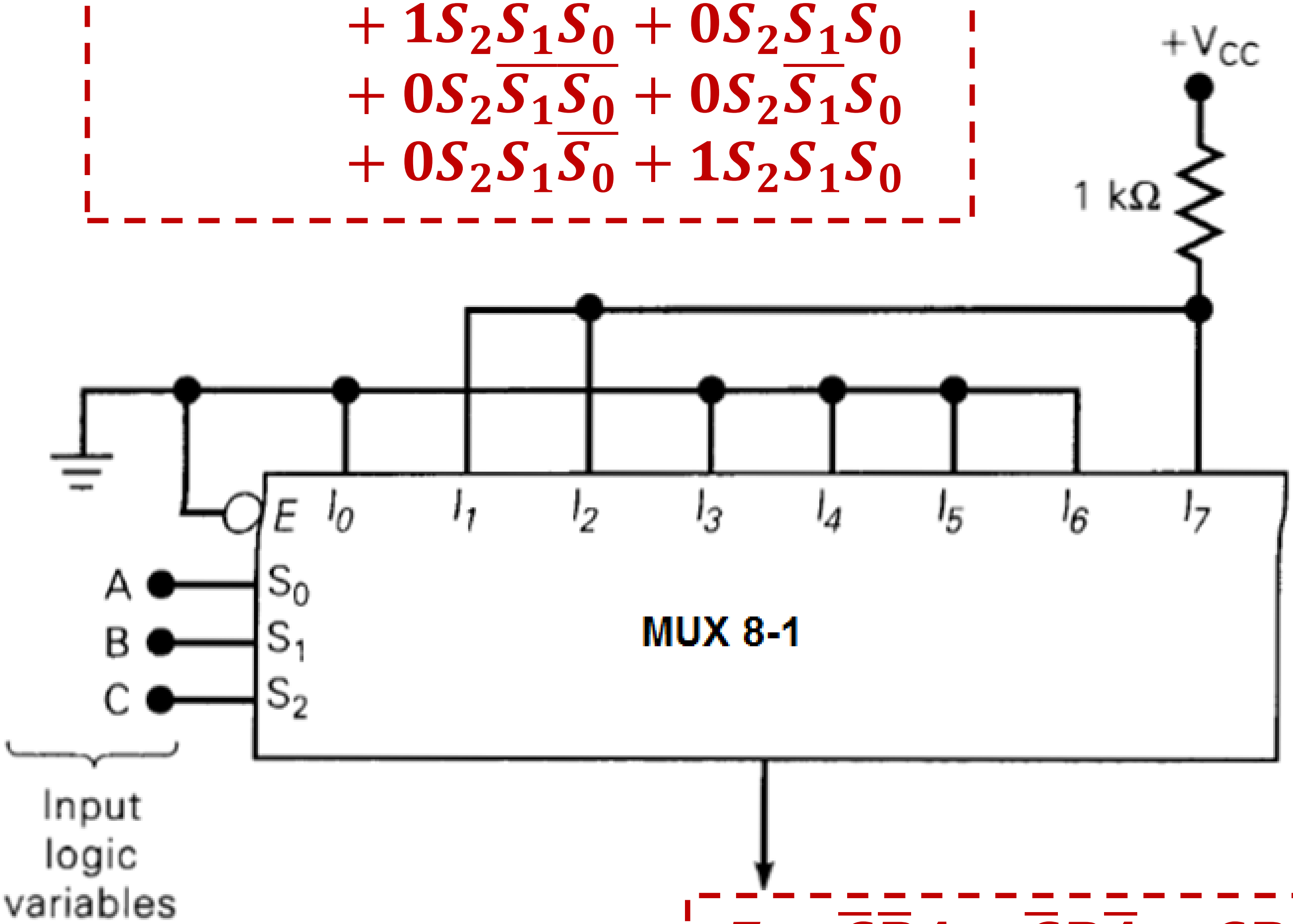


$$Z = I_0\overline{S_2}\,\overline{S_1}\,\overline{S_0} + I_1\overline{S_2}\,\overline{S_1}S_0 + I_2\overline{S_2}S_1\overline{S_0} + I_3\overline{S_2}S_1S_0 + I_4S_2\overline{S_1}\,\overline{S_0} + I_5S_2\overline{S_1}S_0 + I_6S_2S_1\overline{S_0} + I_7S_2S_1S_0$$

Aplicatii MUX-uri: generarea functiilor logice

- Se leaga la 1 intrarile ce corespund mintermenilor doriti

$$
\begin{aligned}
Z = 0\overline{S_2}\,\overline{S_1}\,\overline{S_0} &+ 1\overline{S_2}\,\overline{S_1}S_0 \\
&+ 1\overline{S_2}S_1\overline{S_0} + 0\overline{S_2}S_1S_0 \\
&+ 0S_2\overline{S_1}\,\overline{S_0} + 0S_2\overline{S_1}S_0 \\
&+ 0S_2S_1\overline{S_0} + 1S_2S_1S_0
\end{aligned}
$$

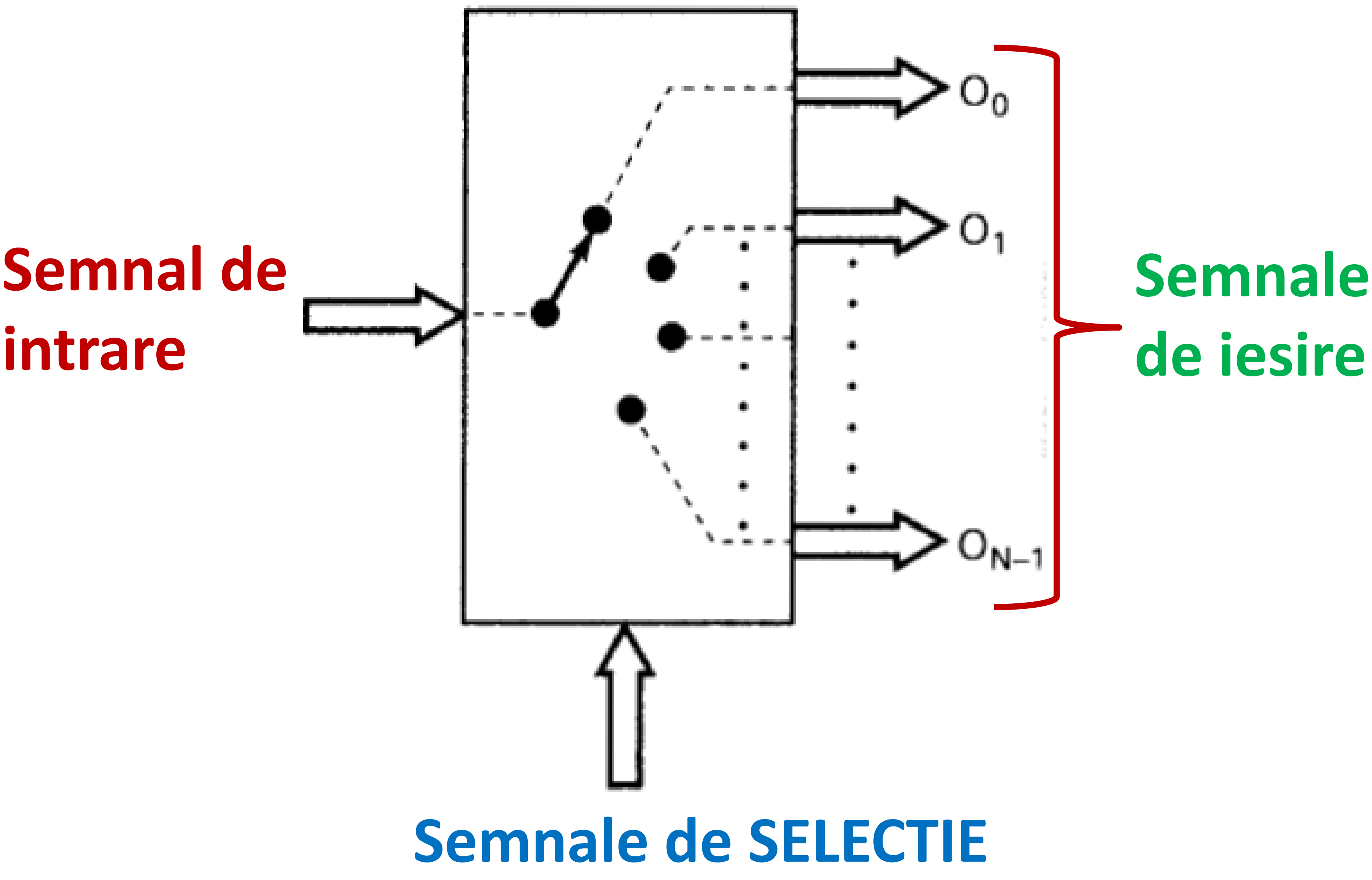


C	B	A	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

$$Z = \overline{C}\,\overline{B}A + \overline{C}B\overline{A} + CBA$$

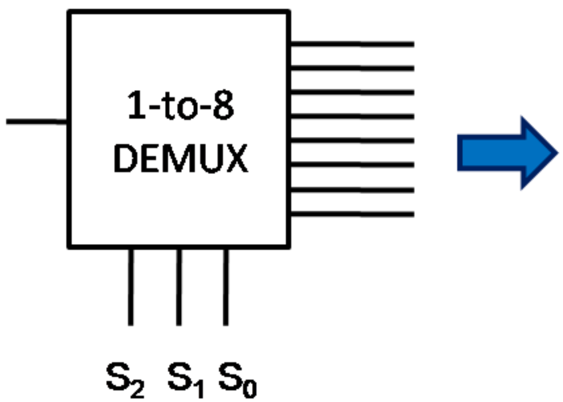
Demultiplexori DEMUX – Data distributors

- Efectueaza operatie inversa MUX

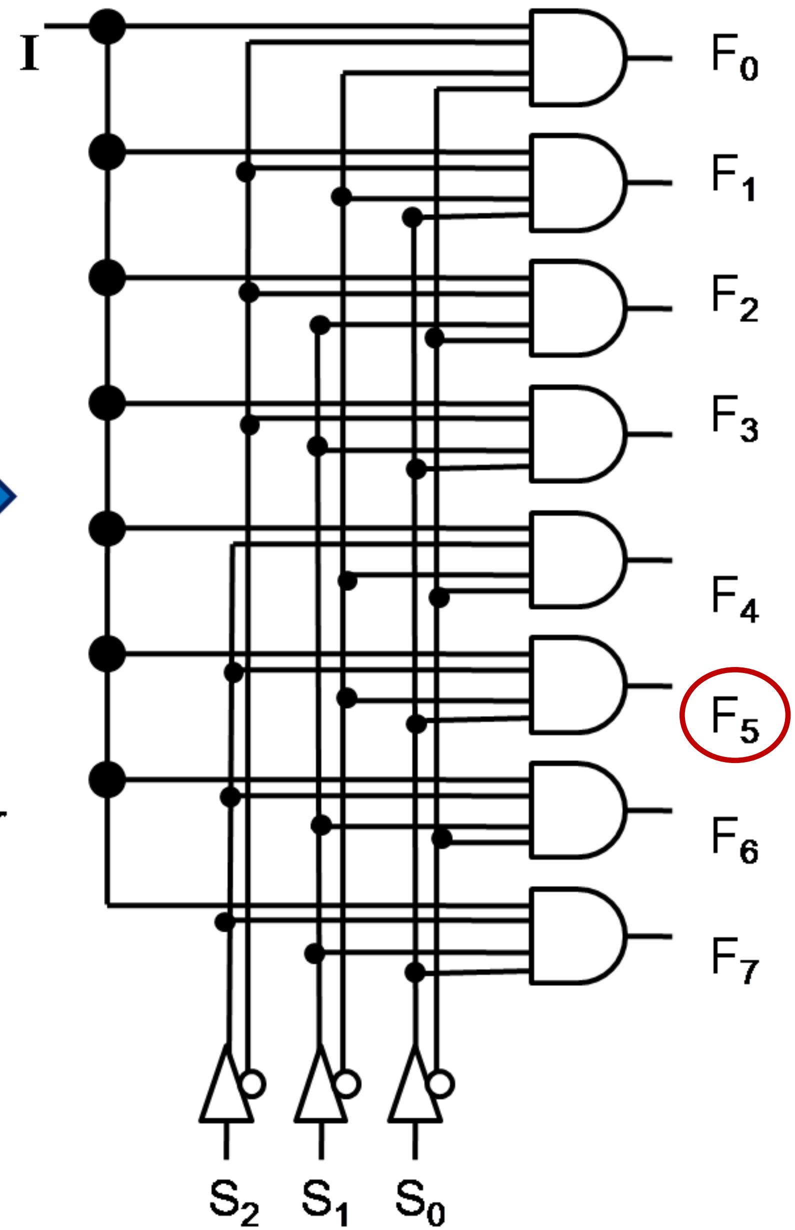


DEMUX: 1 – 8

- Iesirea selectata copiaza intrarea



1-to-8 line demultiplexer



$$F_5 = I \cdot S_2 \cdot \overline{S_1} \cdot S_0$$

Diagrame Karnaugh 3 variabile

- Diagramele Karnaugh (K maps) continua in mod logic diagramele Veitch

Tabela de adevar

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0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Diagrama Karnaugh

		AB			
		00	01	11	10
C	0	0	1	1	0
	1	1	0	0	1

Diagrama Veitch

			A	
	0	1	1	0
C	1	0	0	1
		B		

Diagrame Karnaugh 4 variabile

- Diagramele Karnaugh (K maps) continua in mod logic diagramele Veitch

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0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Diagrama Karnaugh

		AB			
		00	01	11	10
CD	00	1	0	0	1
	01	0	1	1	0
	11	0	1	1	0
	10	1	0	0	1

Diagrama Veitch

			A		
	1	0	0	1	
	0	1	1	0	D
C	0	1	1	0	
	1	0	0	1	
		B			

4 to 2 priority encoder

- O secretara deserveste 4 directori.
- Ea are in birou o centrala telefonica pe care sunt 4 Becuri, cate unul pentru fiecare director.
- Directorii au ranguri diferite. In ordine descrescatoare a rangurilor ei sunt: D3, D2, D1 si D0.
- Daca 2 (sau mai multi) directori solicita simultan un serviciu de la secretara (fiecare apasand butonul din biroul sau) pe panoul secretarei se va aprinde doar becul directorului cel mai mare in rang dintre solicitatori.

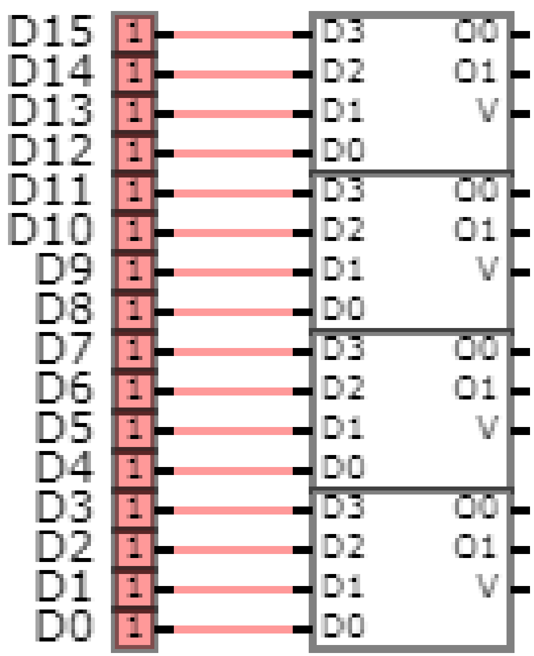
Codul celui mai mare in rang

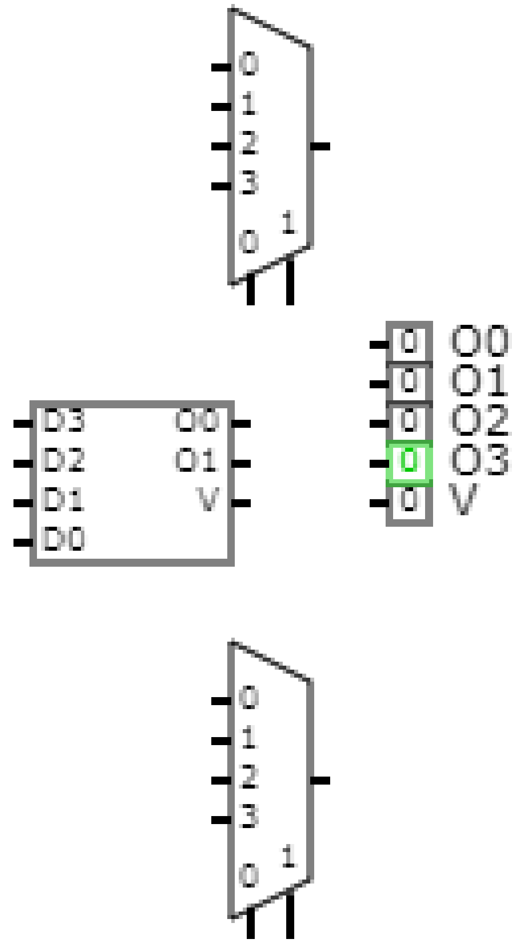
Exista solicitare ?

D3	D2	D1	D0	O_1	0_0	V
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

Tema acasa: PE 16-4

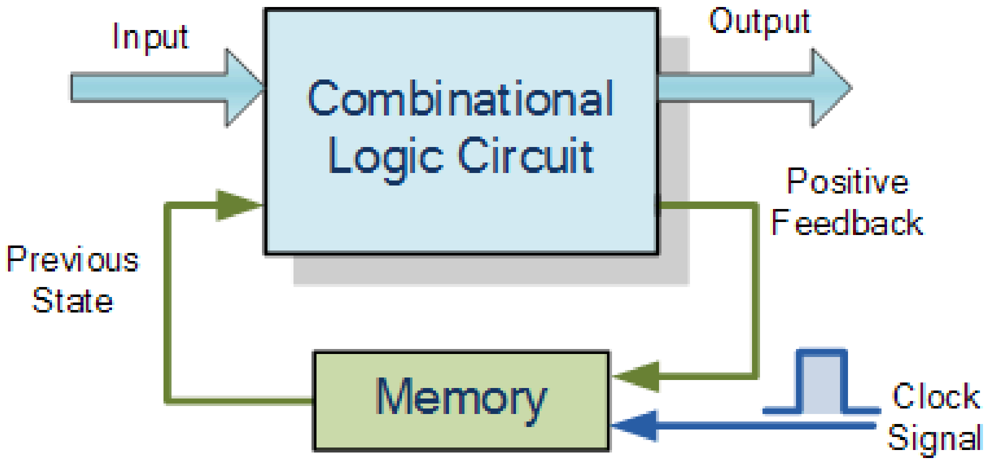
- **Folosind 5 * PE 4-2 , 2* MUX-uri 4-1 implementati un PE 16-4.**
- **Folosind un DEMUX 1-16 verificati functionarea corecta a PE 16-4.**





Circuite logice Secventiale

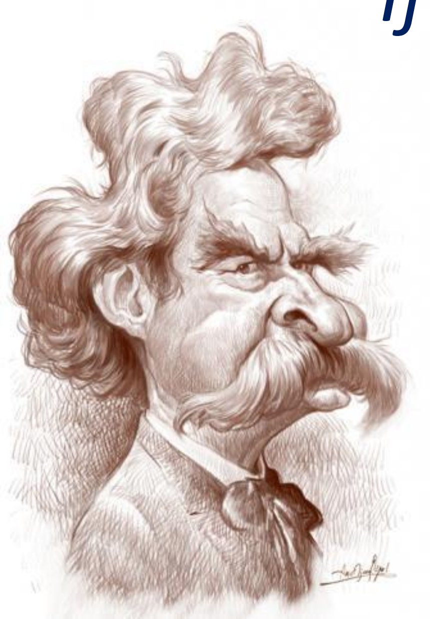
In digital **circuit** theory, **sequential logic** is a type of **logic circuit** whose output depends not only on the present value of its input signals but on the sequence of past inputs, the input history. This is in contrast to combinational **logic**, whose output is a function of only the present input.



Circuite Logice Secventiale

"If you tell the truth, you don't have to remember anything."

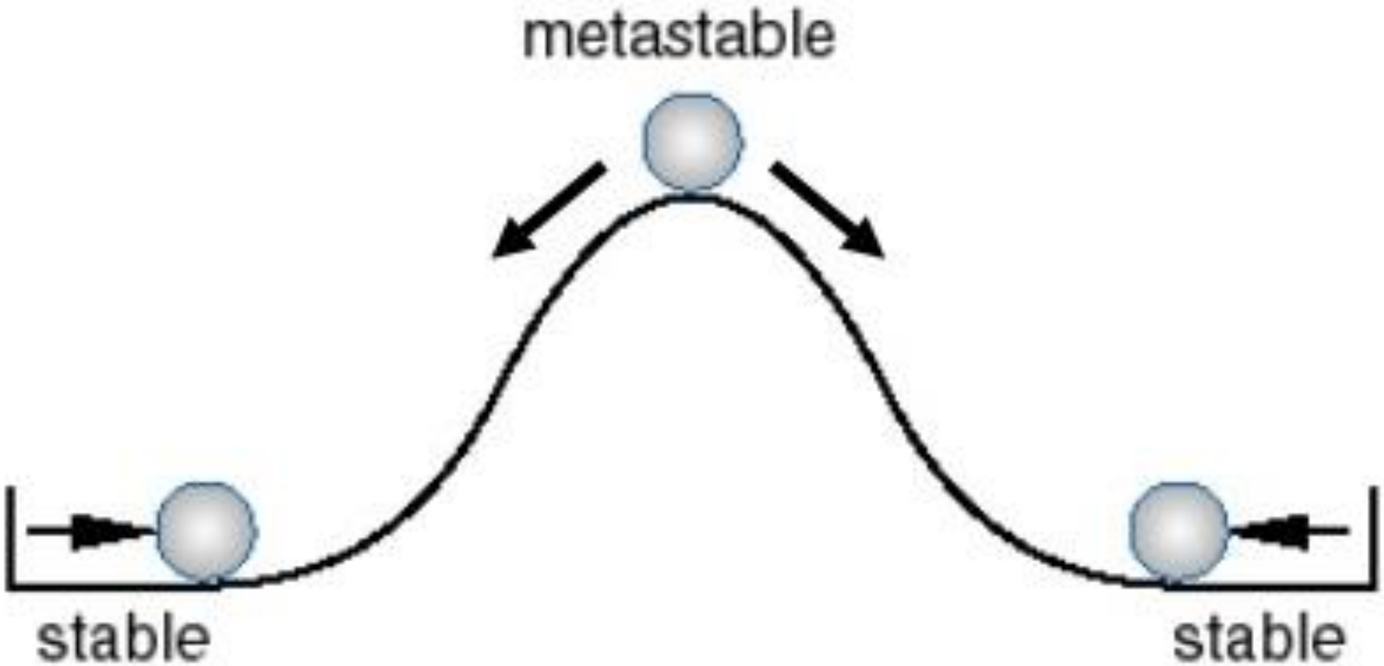
— Mark Twain —



Bistabilii

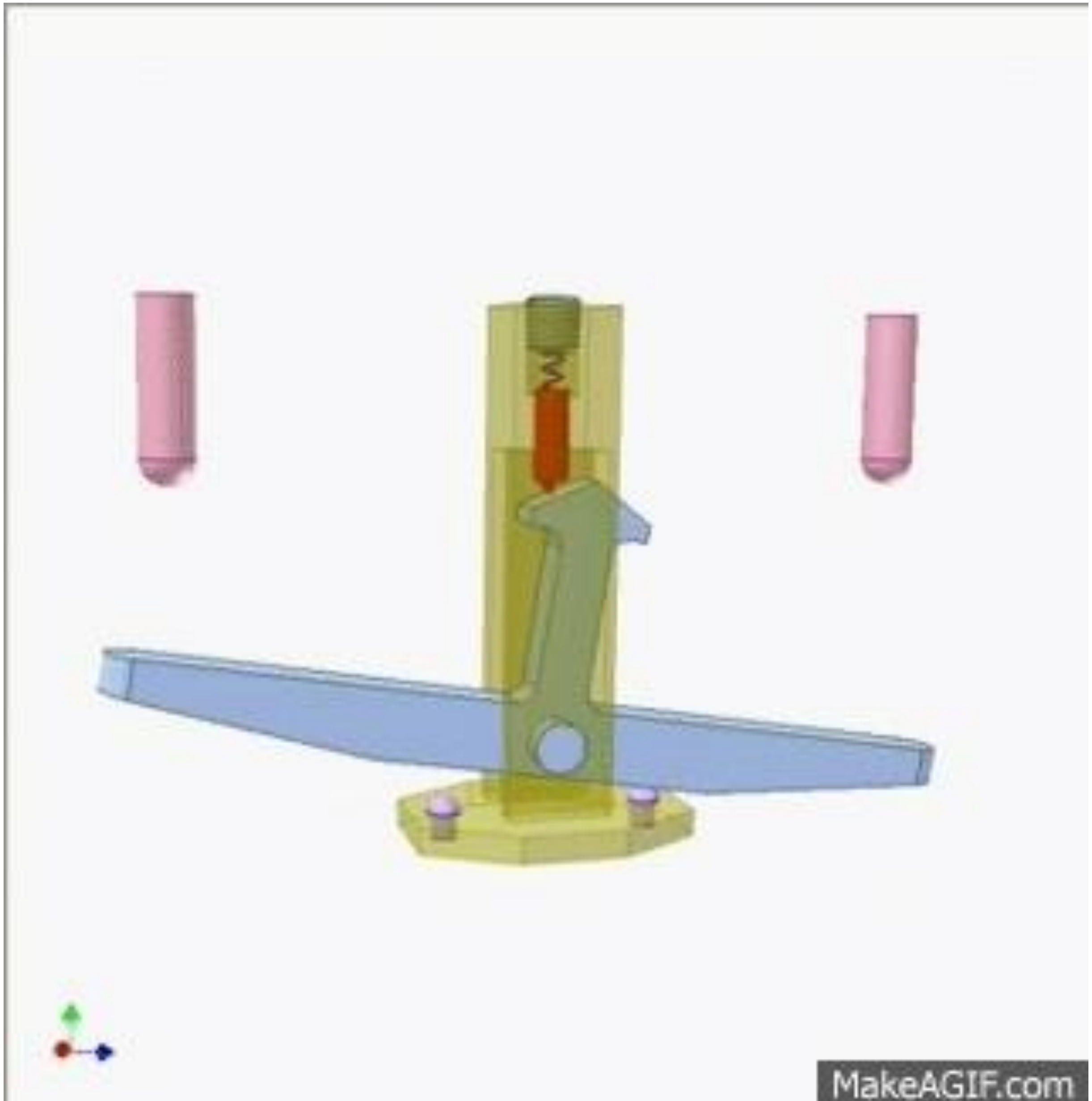
Stabilitate - Instabilitate

- Another mechanical analogy for metastability

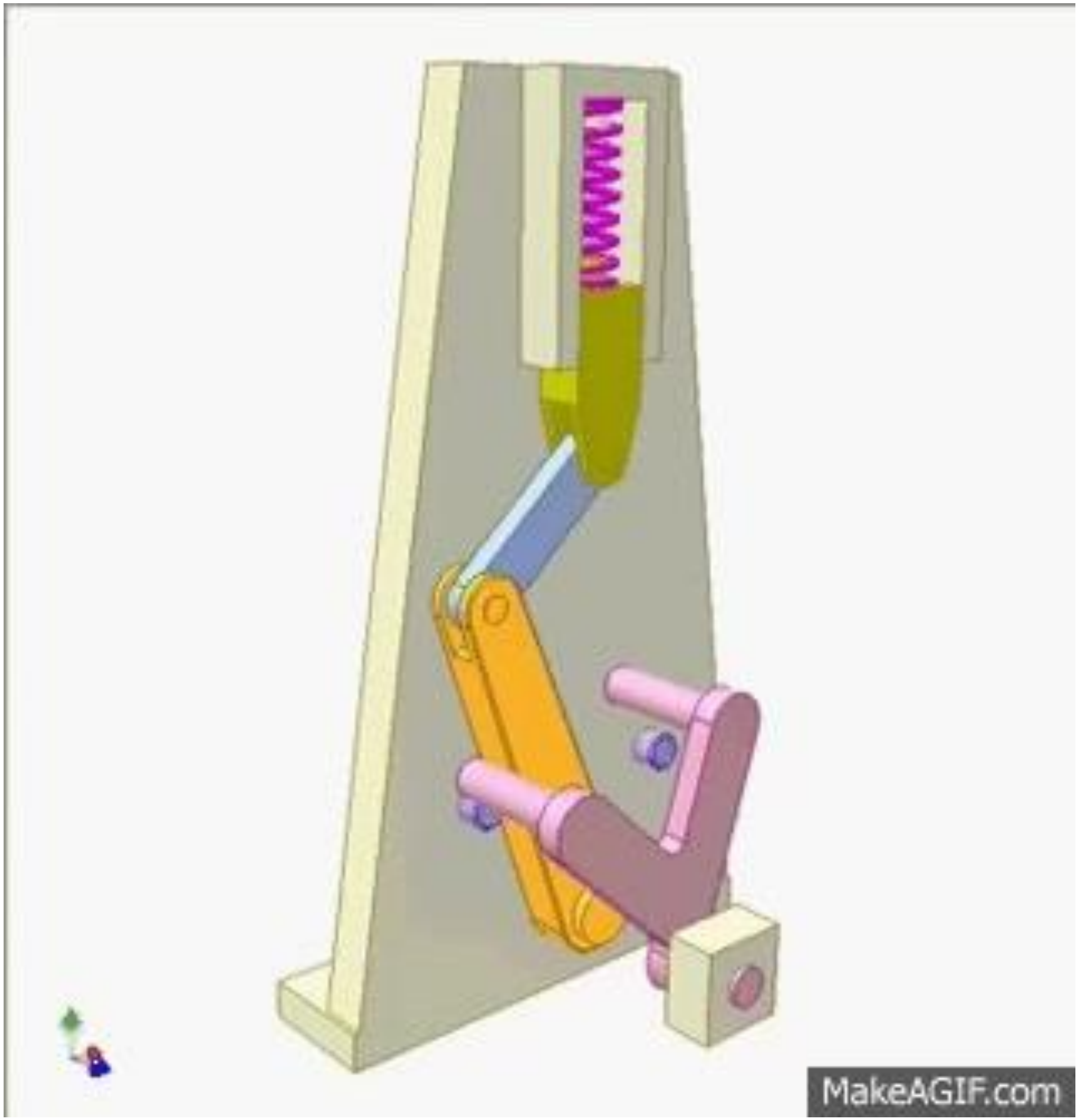


A small movement from metastability leads to stability.

Stabilitate - Instabilitate



Stabilitate - Instabilitate

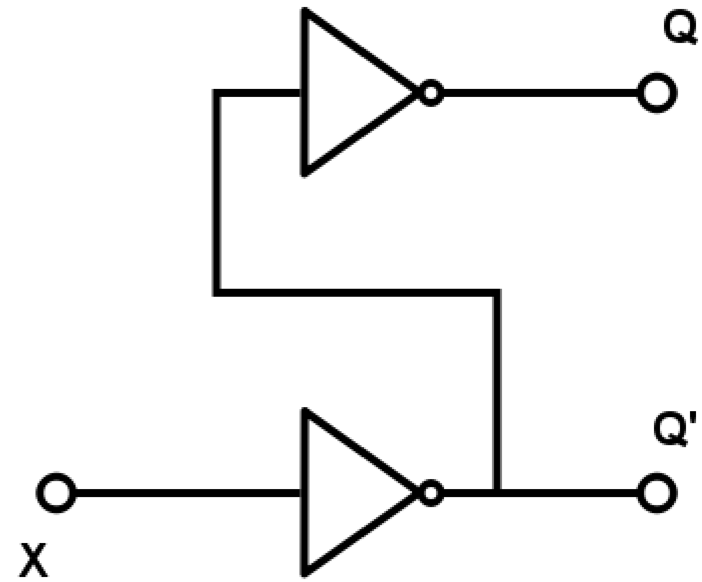


Stabilitate - Instabilitate

Bistabili

- Cum obtinem un Bistabil?

Fie circuitul: $Q' = \bar{X}, Q = \bar{\bar{X}}$



Adaugam legatura

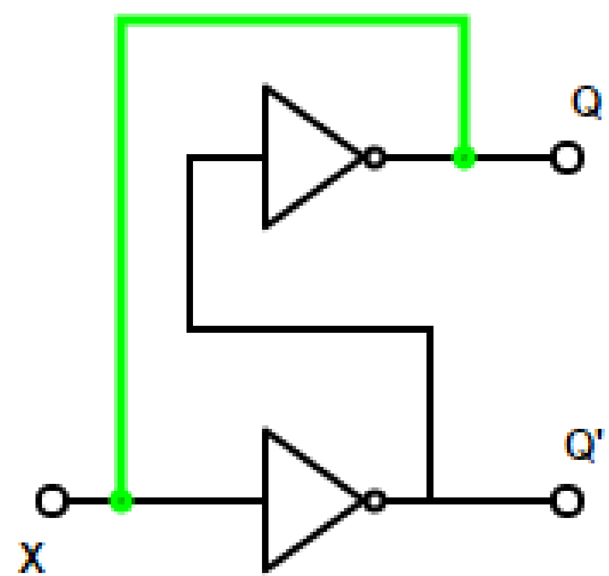
de la iesire la intrare $Q \rightarrow X$.

Acest circuit NU ARE NEVOIE

DE SEMNAL DE INTRARE !!!

Circuitul are 2 solutii logice:

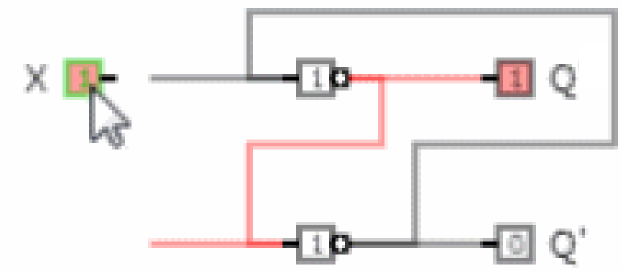
1. $Q = 1; Q' = 0$ si respectiv
2. $Q = 0; Q' = 1$



Bistabilul simulat in wronex

- Cum obtinem un Bistabil?

Fie circuitul: $Q' = \bar{X}, Q = \bar{\bar{X}}$



Adaugam legatura

de la iesire la intrare $Q \rightarrow X$.

Acest circuit NU ARE NEVOIE DE SEMNAL DE INTRARE !!!

Circuitul are 2 solutii logice:

1. $Q = 1; Q' = 0$ si respectiv
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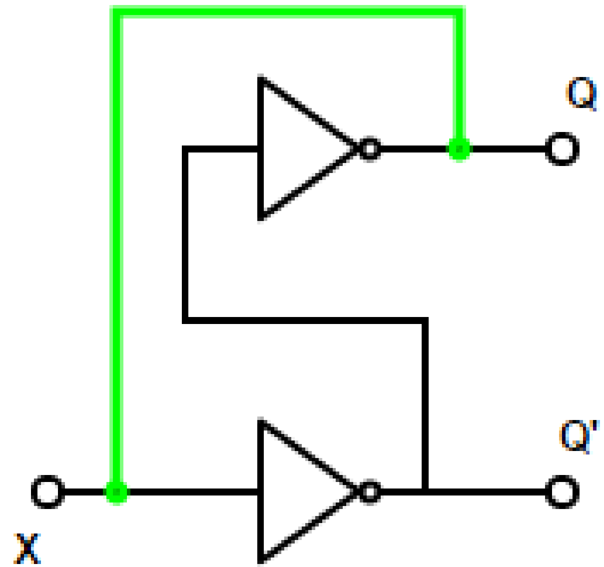
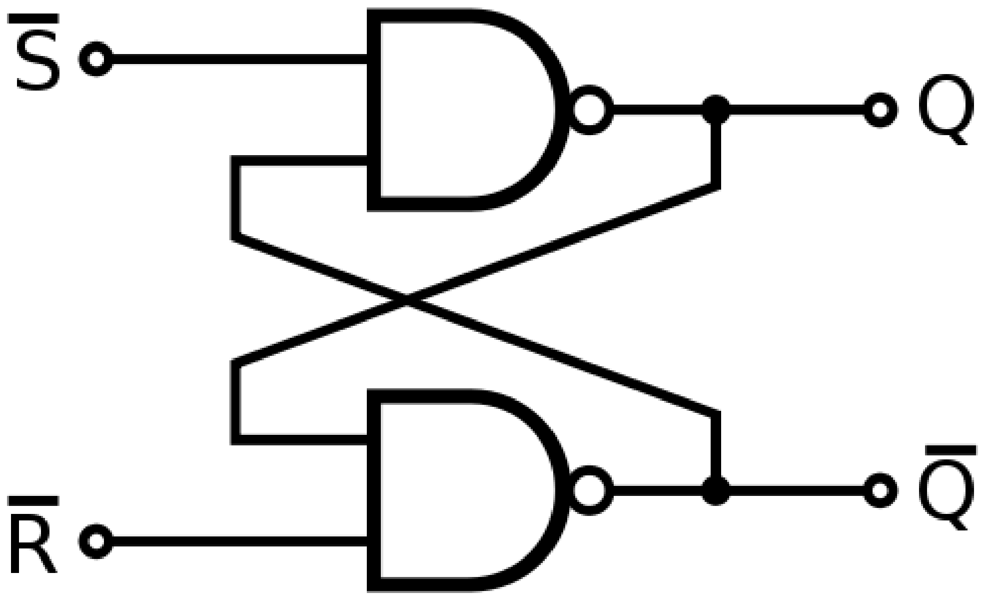
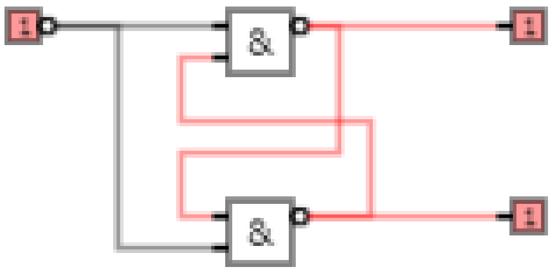
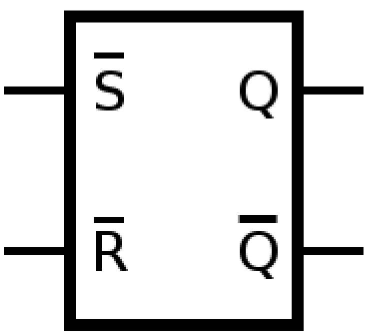


BB : NAND LATCH — SR NAND LATCH

- **Memoreaza atunci cand ambele intrari sunt in 1**
- **Ambele intrari in 0 forteaza iesirile in 1**
- **Trecerea simultana a intrarilor din 0 in 1 (L→H) ➔poate produce oscilatii (TEMA: de verificat in WRONEX)**



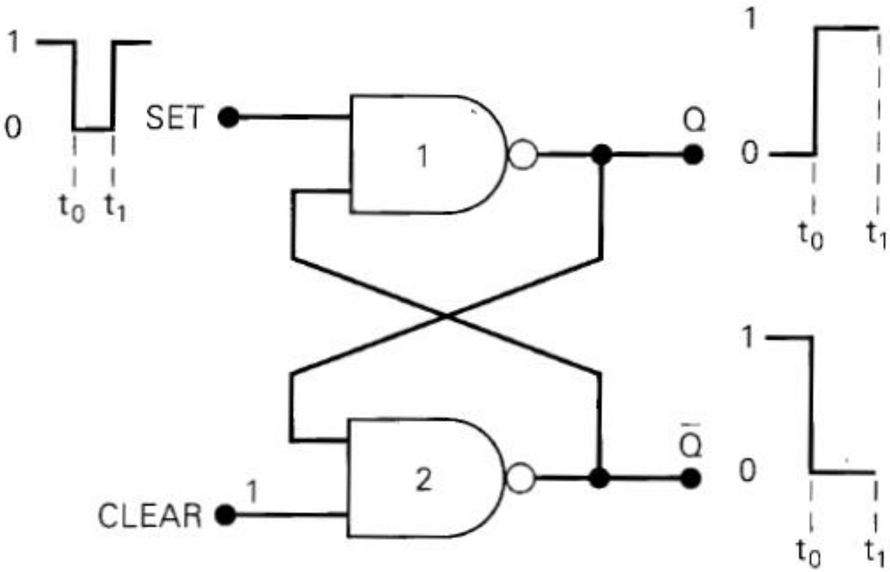


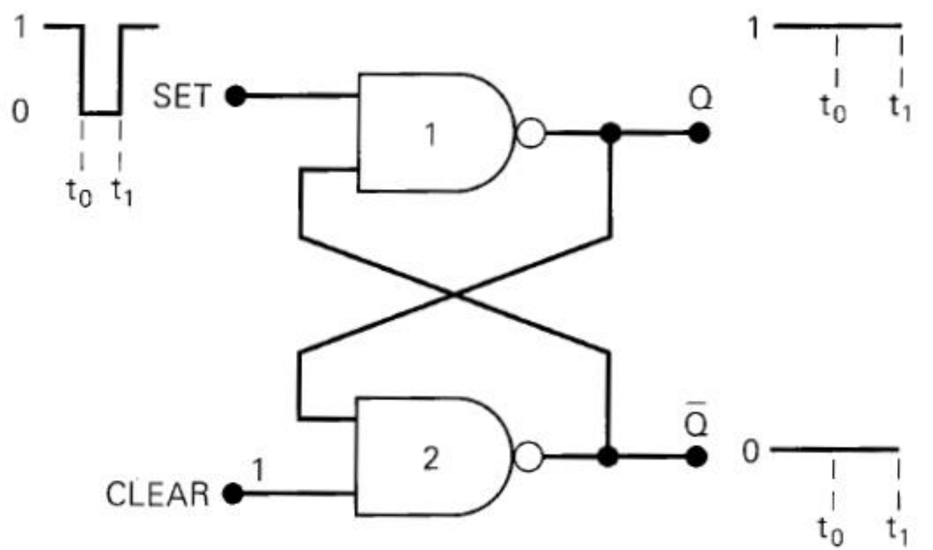


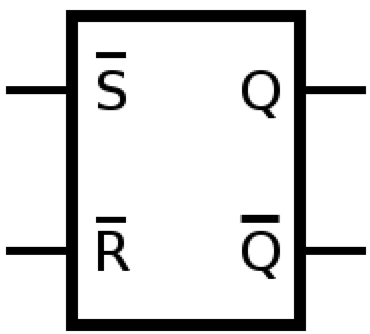
In practica, datorita inegalitatii timpilor de propagare oscilatia inceteaza dupa cateva perioade

Bistabilul : **NAND** LATCH — SETAREA

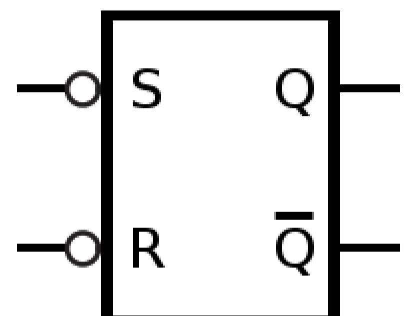
- **Setarea/Resetare se face prin aducerea in stare LOW a intrarii corespunzatoare → Intrari active LOW**





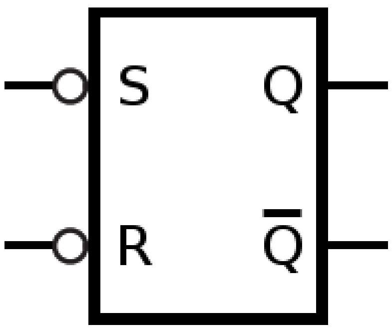


sau



Bistabilul : NAND LATCH — Tabela

- Memoreaza atunci cand ambele intrari sunt in 1
- Ambele intrari in 0 forteaza iesirile in 1 ->INTERZISA
- Setarea/Resetare se face prin aducerea in stare LOW a intrarii corespunzatoare ➔ Intrari active LOW

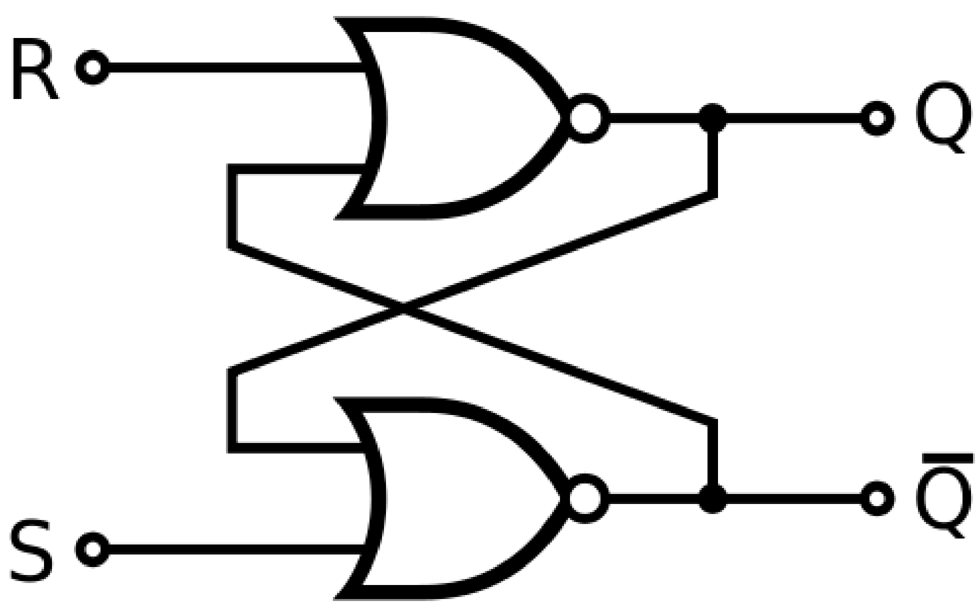


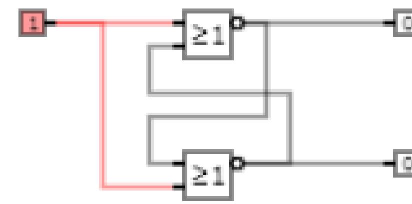
Set	Clear	Output	
1	1	No change	Memoreaza
0	1	Q = 1	SET
1	0	Q = 0	RESET
0	0	Invalid*	Interzisa

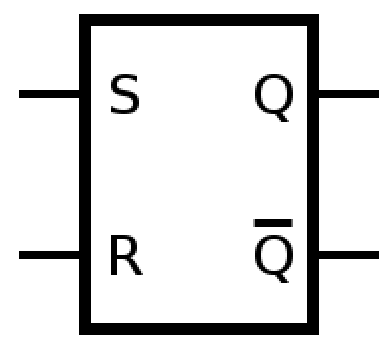
*produces $Q = \overline{Q} = 1$

BB : NOR LATCH —SR NOR LATCH

- Memoreaza atunci cand ambele intrari sunt in 0
- Ambele intrari in 1 forteaza iesirile in 0
- Trecerea simultana a intrarilor din 1 in 0 (H→L) →poate produce oscilatii (TEMA: de verificat in WRONEX)



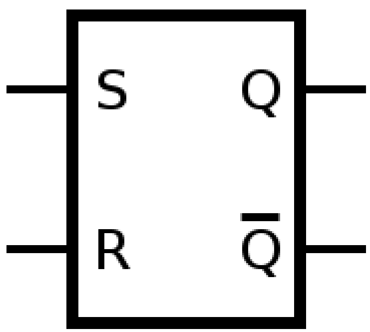


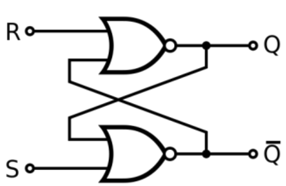


In practica, datorita inegalitatii timpilor de propagare oscilatia inceteaza dupa cateva perioade

Bistabilul : SR NOR LATCH

- Memoreaza atunci cand ambele intrari sunt in 0
- Ambele intrari in 1 forteaza iesirile in 0
- Trecerea simultana a intrarilor din 1 in 0 (H→L) →poate produce oscilatii





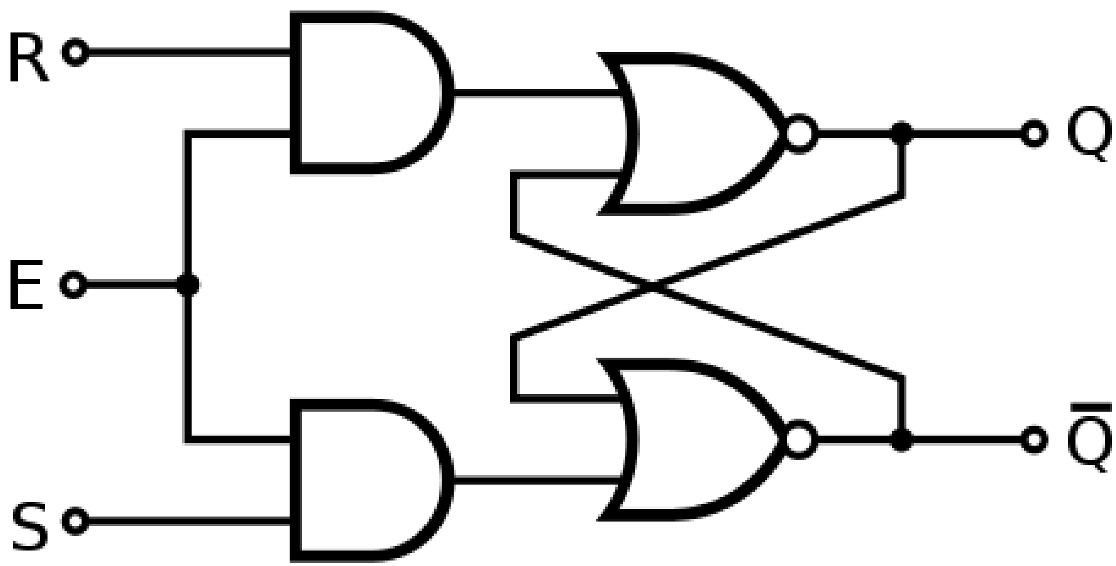
S	R	Q	$\overline{Q}$
0	0	Memorare	
0	1	0	1
1	0	1	0
1	1	Interzisa	

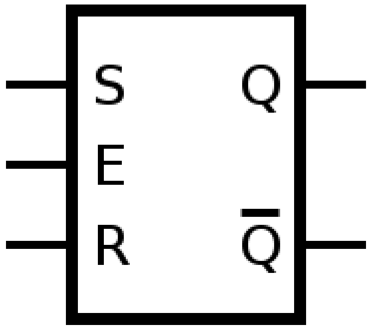
S	R	Q	$\overline{Q}$
0	0	LATCH	
0	1	0	1
1	0	1	0
1	1	Metastable	

Deoarece produce rezultate/stari imprevizibile la trecerea din SR=11 in SR=00

Clocked SR Flip-Flop: Gated SR NOR latch

- Intrarea E-Enable (sau C-CLOCK) permite mai curand selectia bistabilului, decat introducerea functiei de sincronizare dorita.

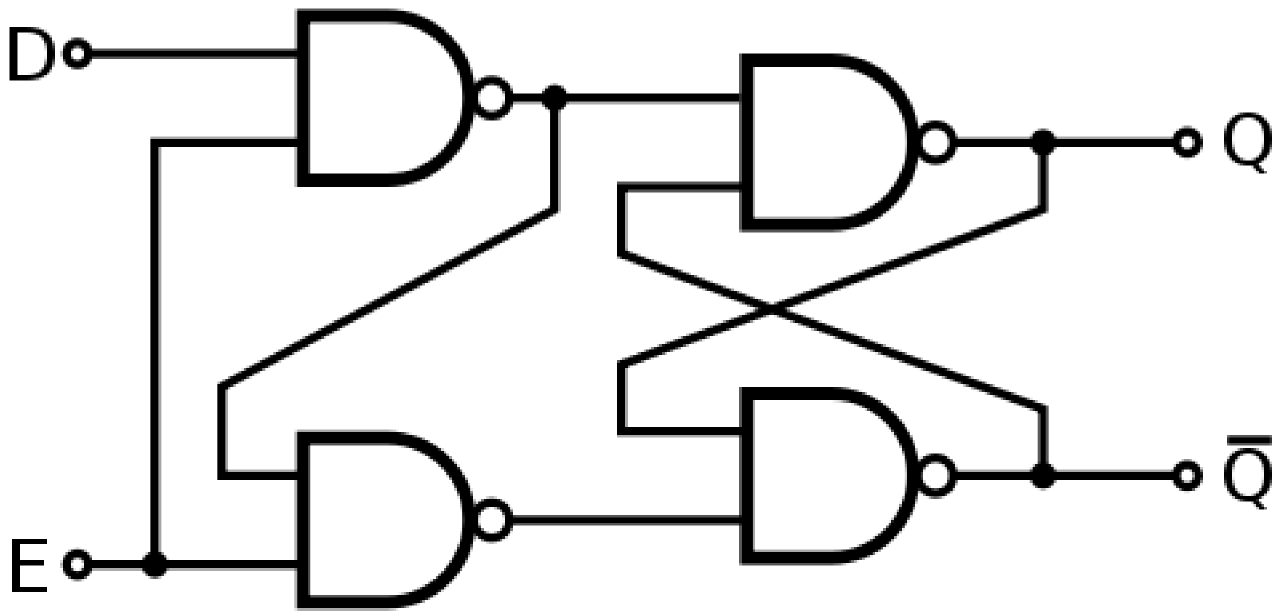




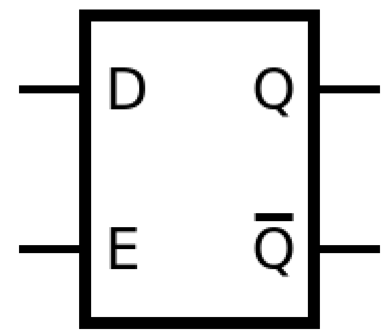
- Aceste LATCH-uri devin "transparente" (iesirea "copiaza" cu starea intrarii) atunci cand intrare E este in stare HIGH. Mai precis: **E=H si R=$\overline{S}$ → Q=S**

Gated D latch based on SR NAND

Transparent LATCH



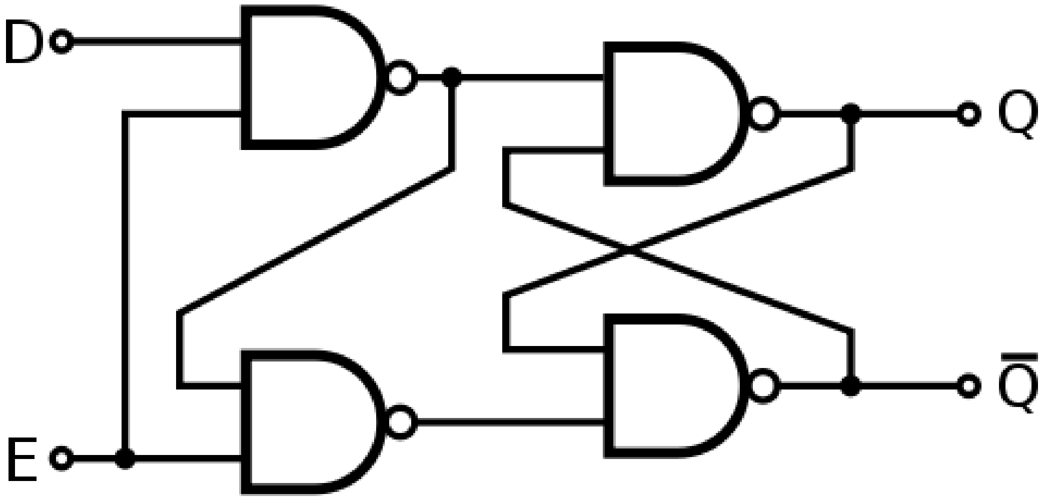
E/C	D		Q	Q'	Comment
0	X		Q_{ant}	$!Q_{ant}$	Mem
1	0		0	1	Reset
1	1		1	0	Set

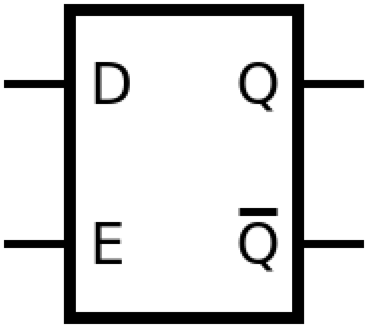


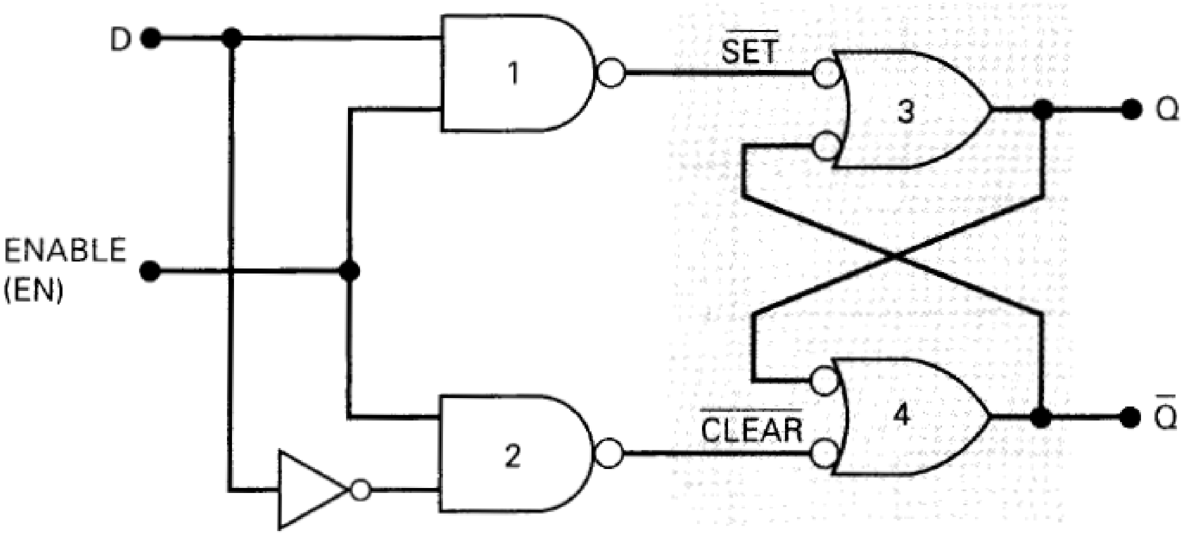
Tema: De simulat in Wronex

De comparat cele doua LATCH-uri

Transparent LATCH



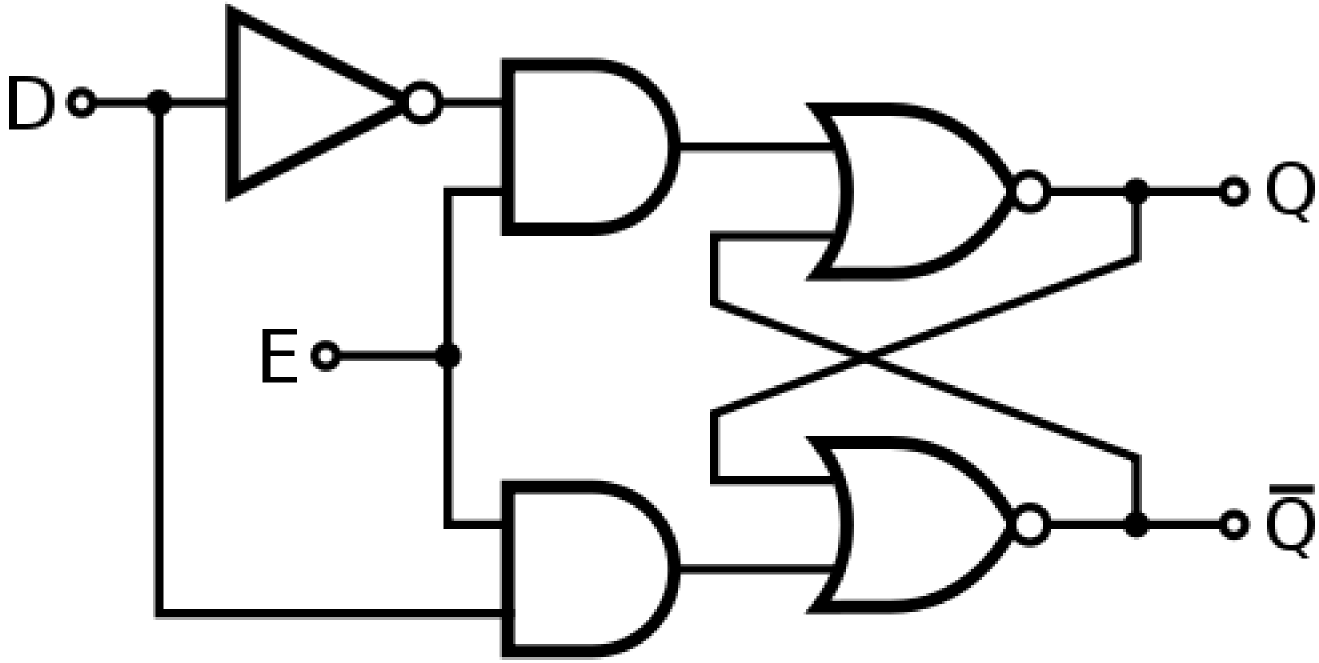




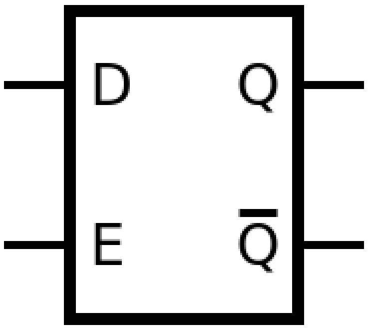
Tema: De simulat in Wronex

Gated D latch based on SR NOR

Transparent D LATCH

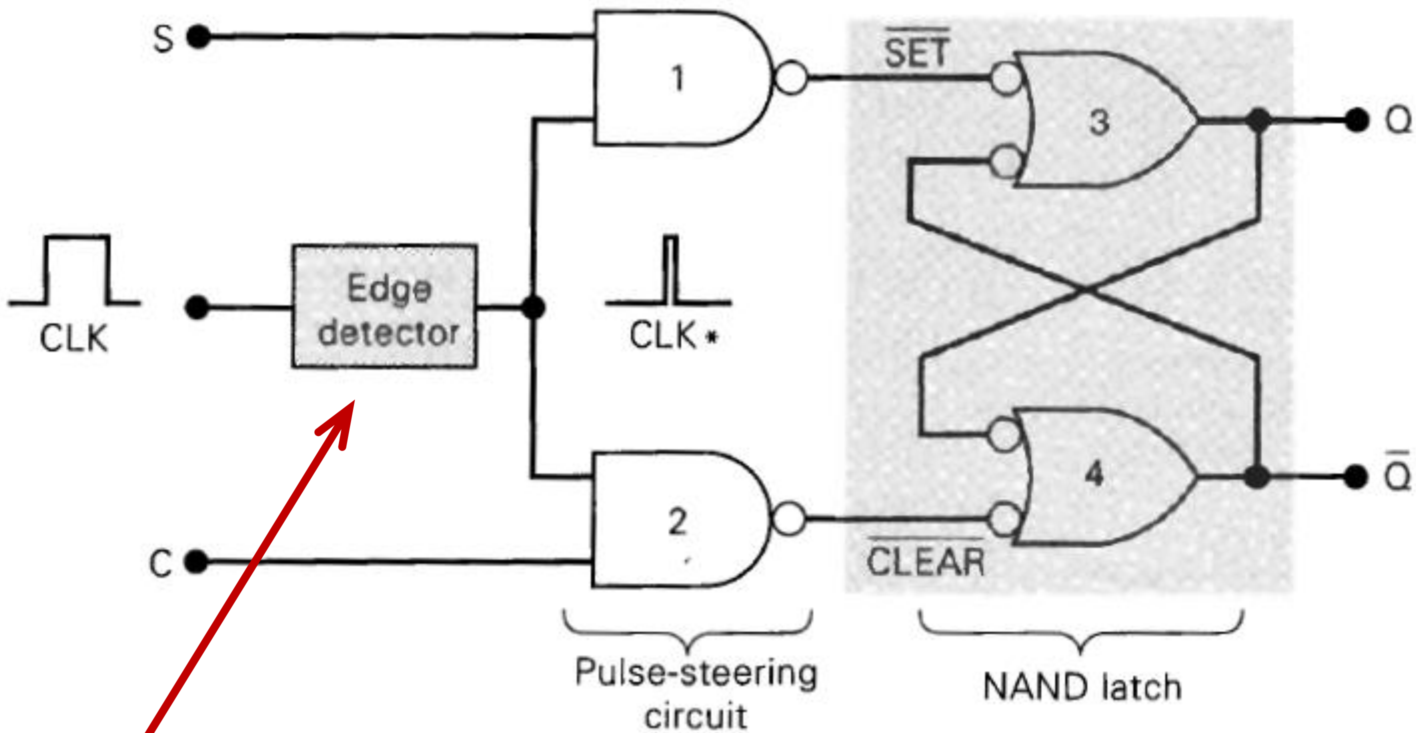


E/C	D		Q	Q'	Comment
0	X		Q_{ant}	$!Q_{ant}$	Mem
1	0		0	1	Reset
1	1		1	0	Set



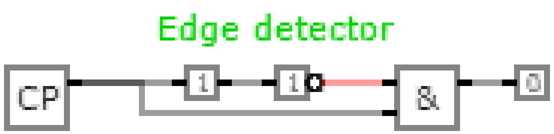
Tema: De simulat in Wronex

Edge Triggered SR Flip-Flop



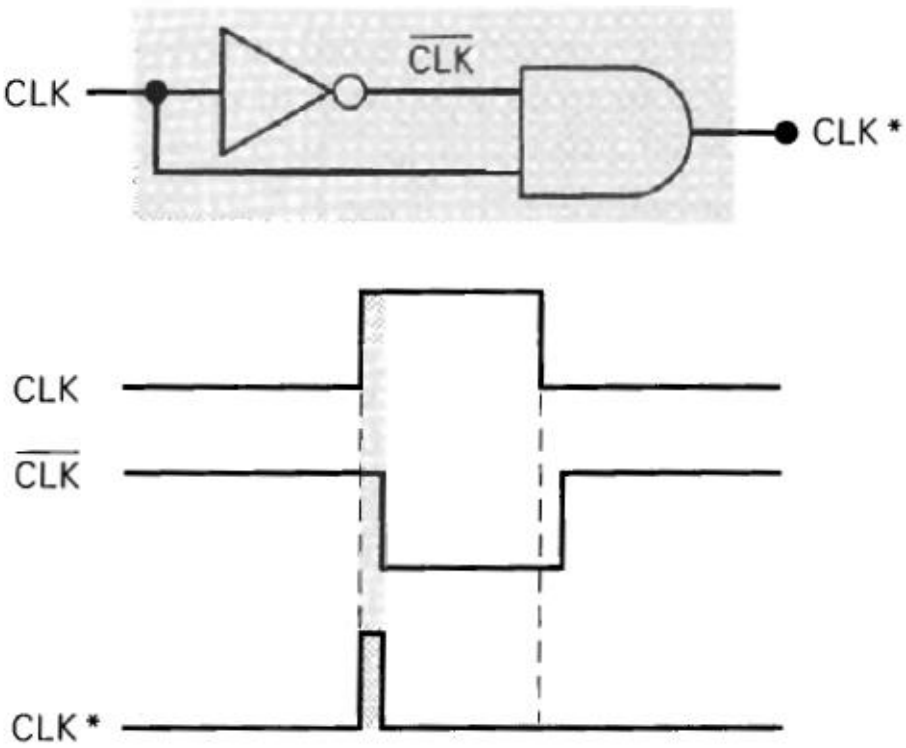
Detector de front

Circuit de dirijare a pulsului

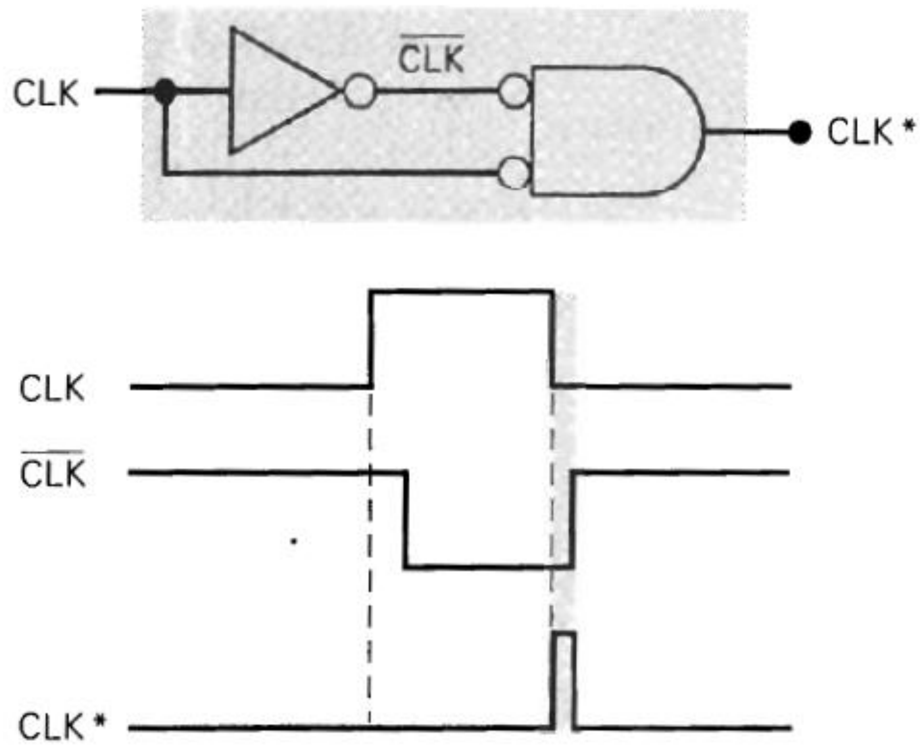


Tema: De simulat in Wronex toata schema

Circuitul Detector de front

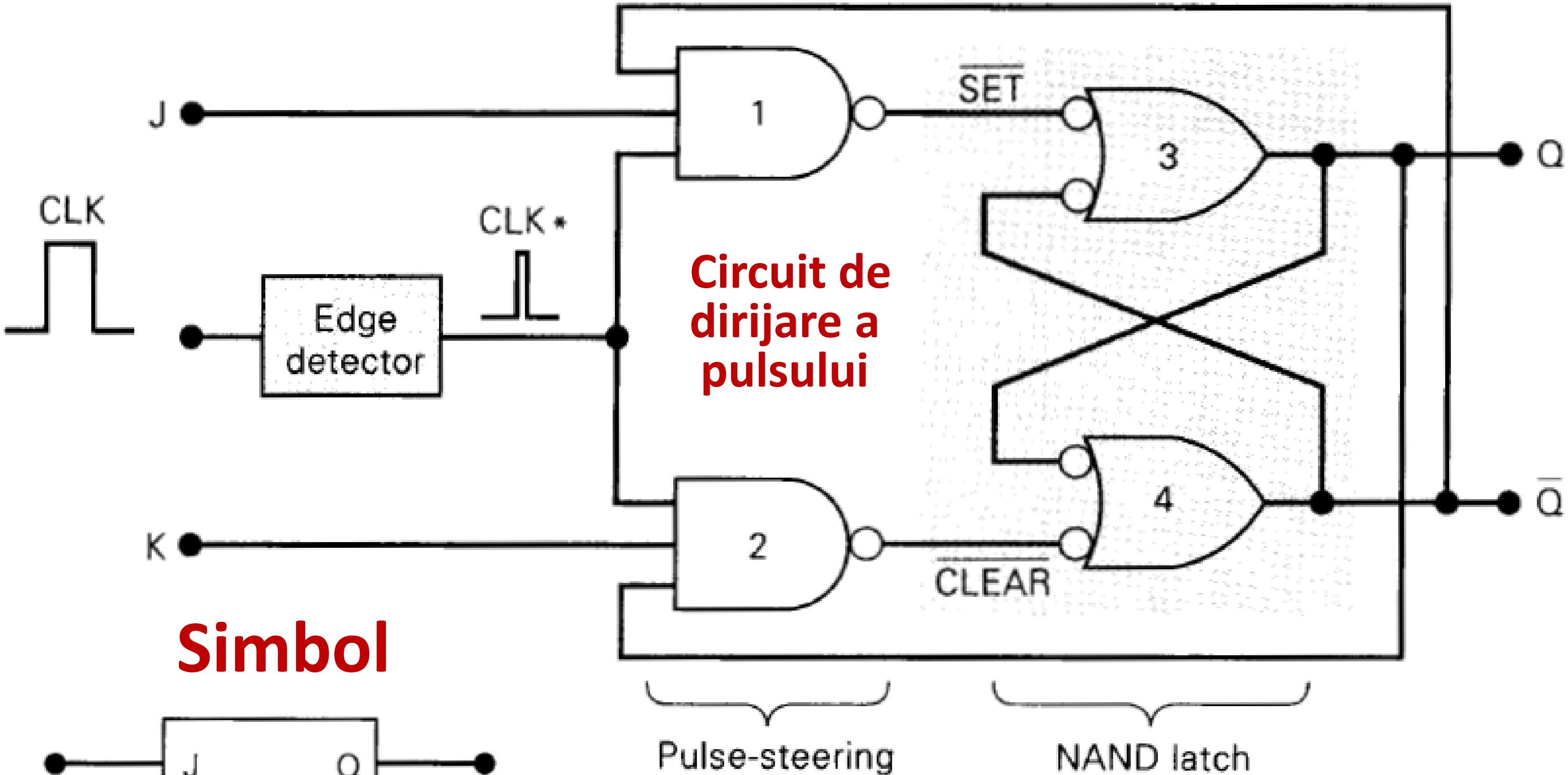


Detector de front pozitiv

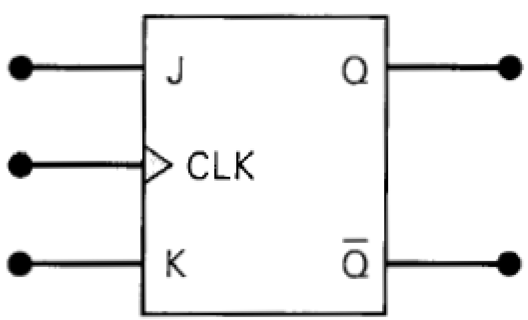


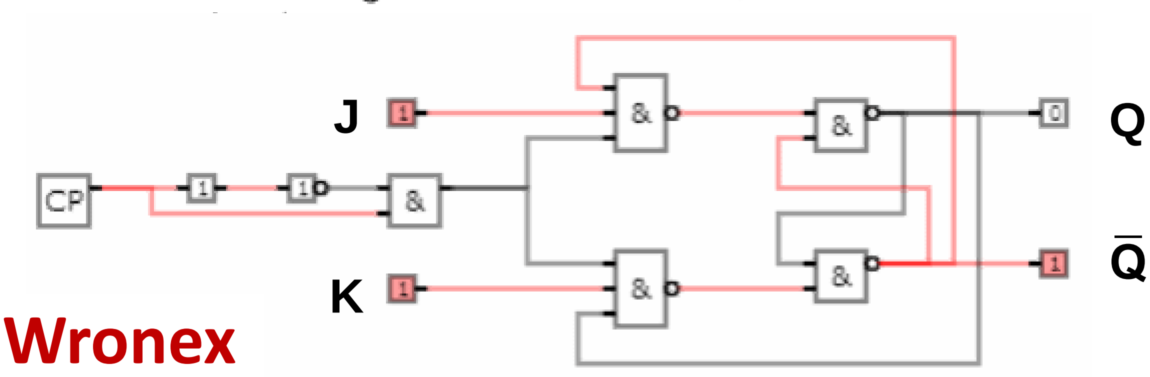
Detector de front negativ

Bistabilul JK: schema interna



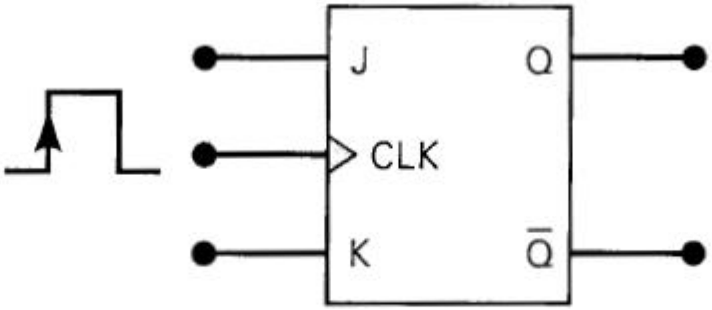
Simbol



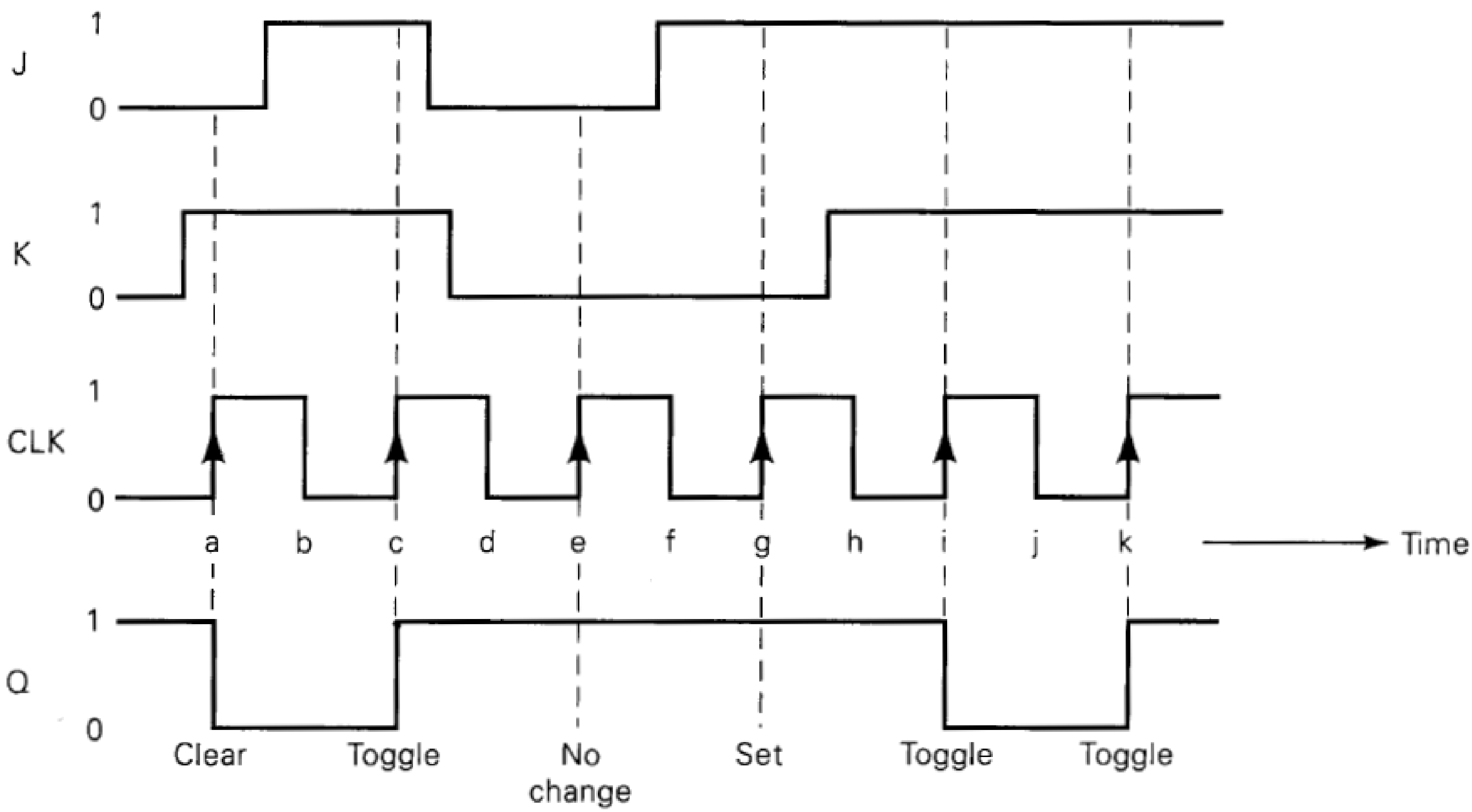


Tema: **De simulat in Wronex**

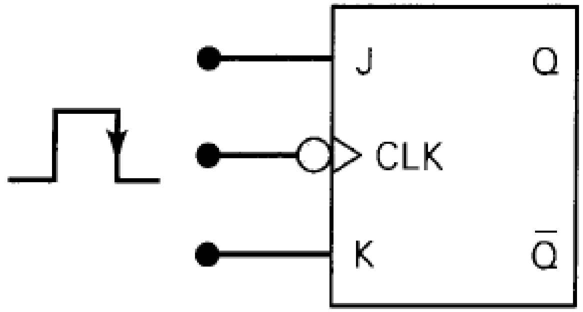
Bistabilul JK: tranzitie pe frontul pozitiv



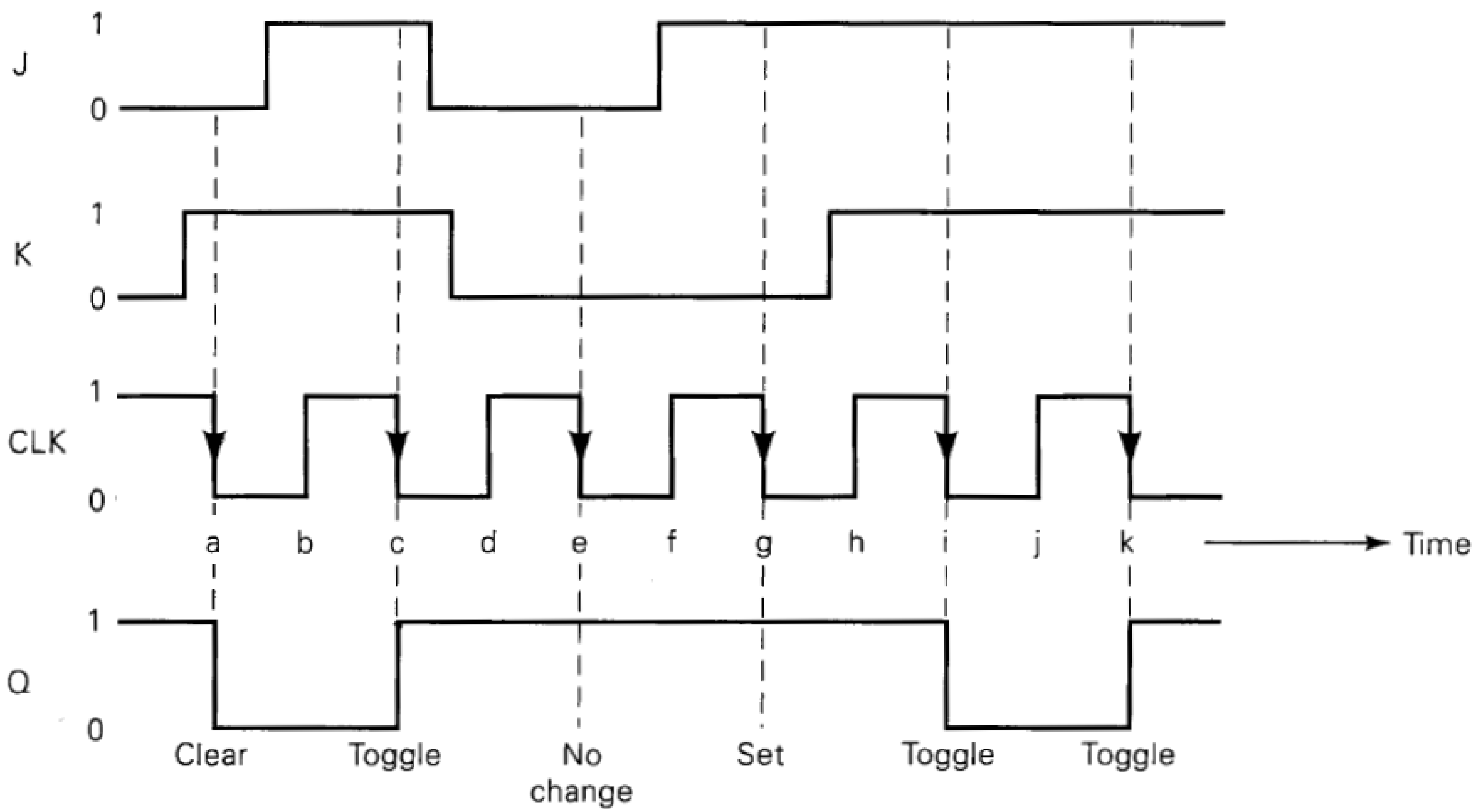
J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)



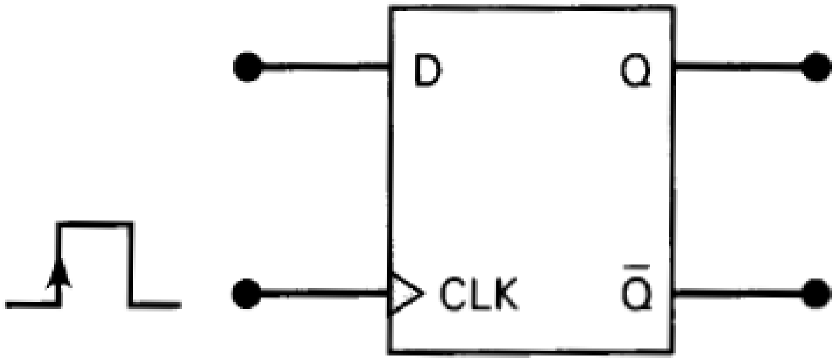
Bistabilul JK: tranzitie pe frontul negativ*



J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q}_0$ (toggles)

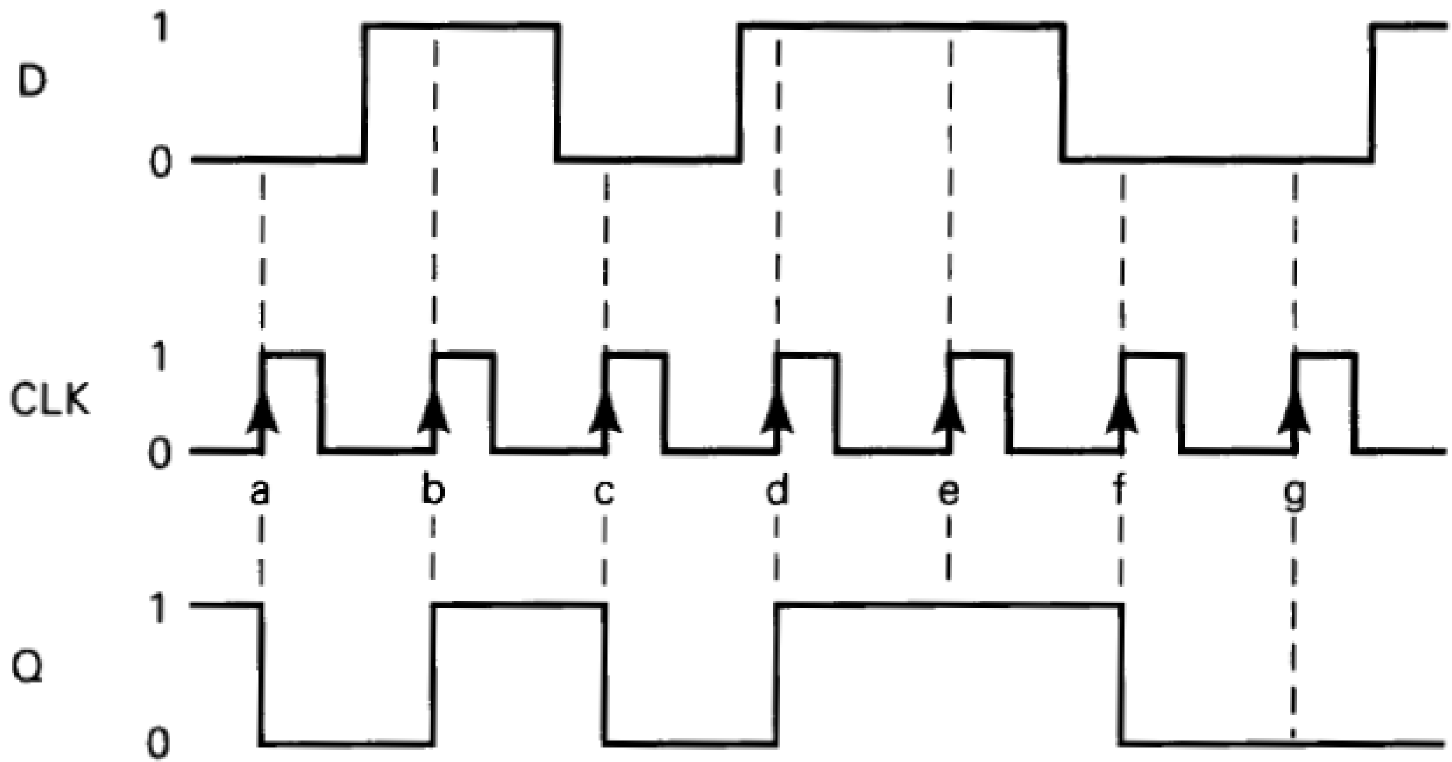


Bistabilul de tip D: *Clocked D Flip-Flop*



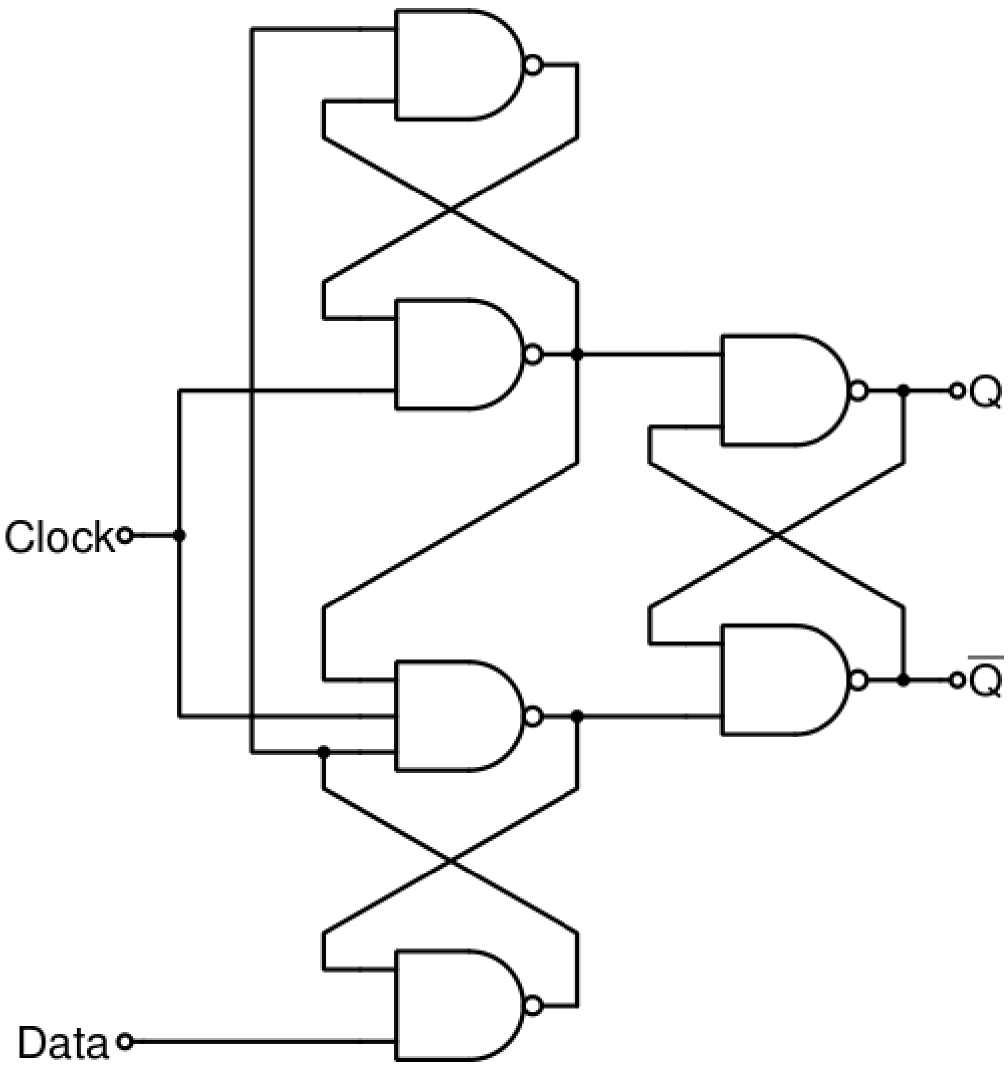
D	CLK	Q
0	↑	0
1	↑	1

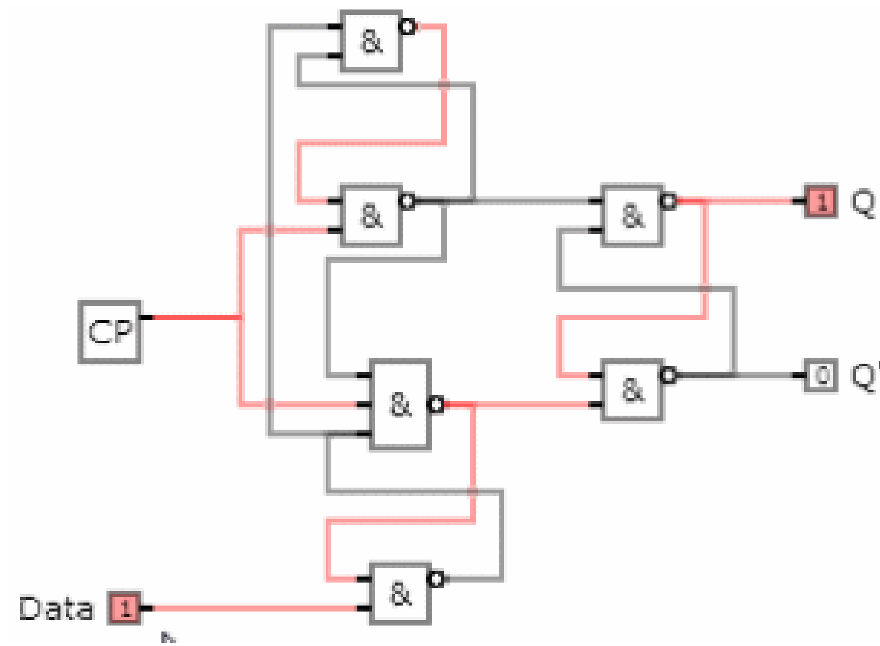
(a)



Bistabilul de tip D: schema interna

Tema: De simulat in Wronex





Multumesc pentru atentie