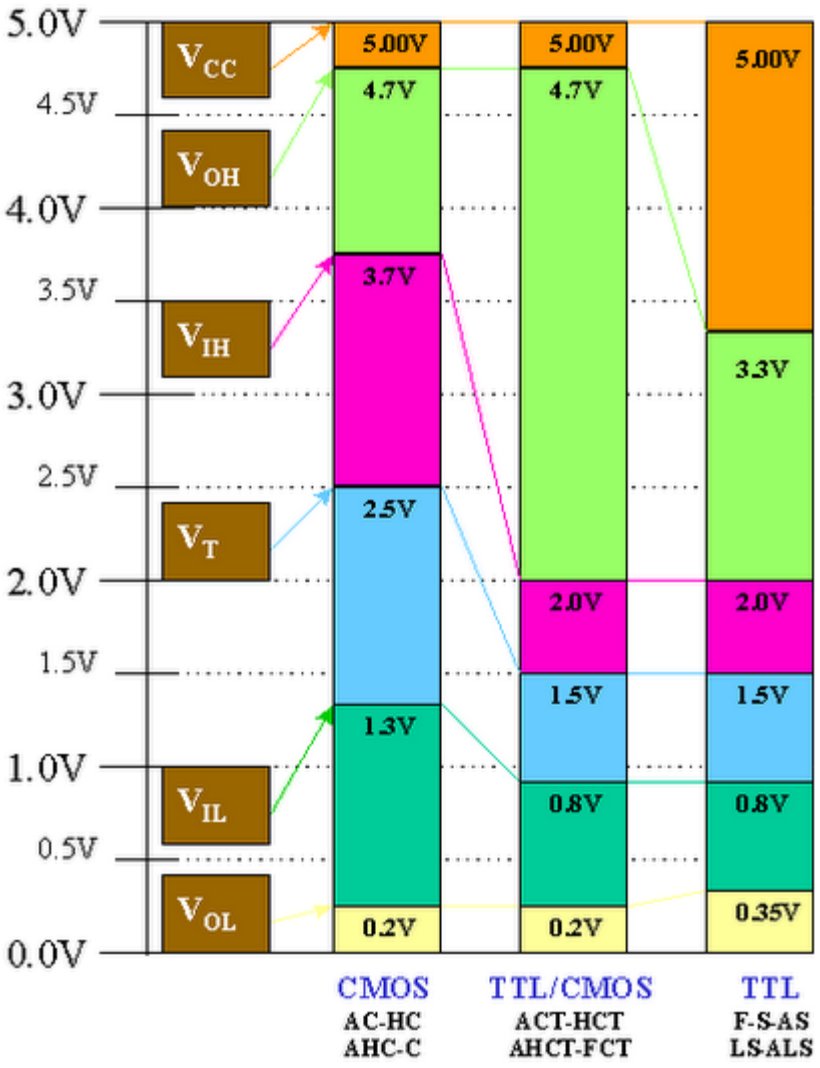
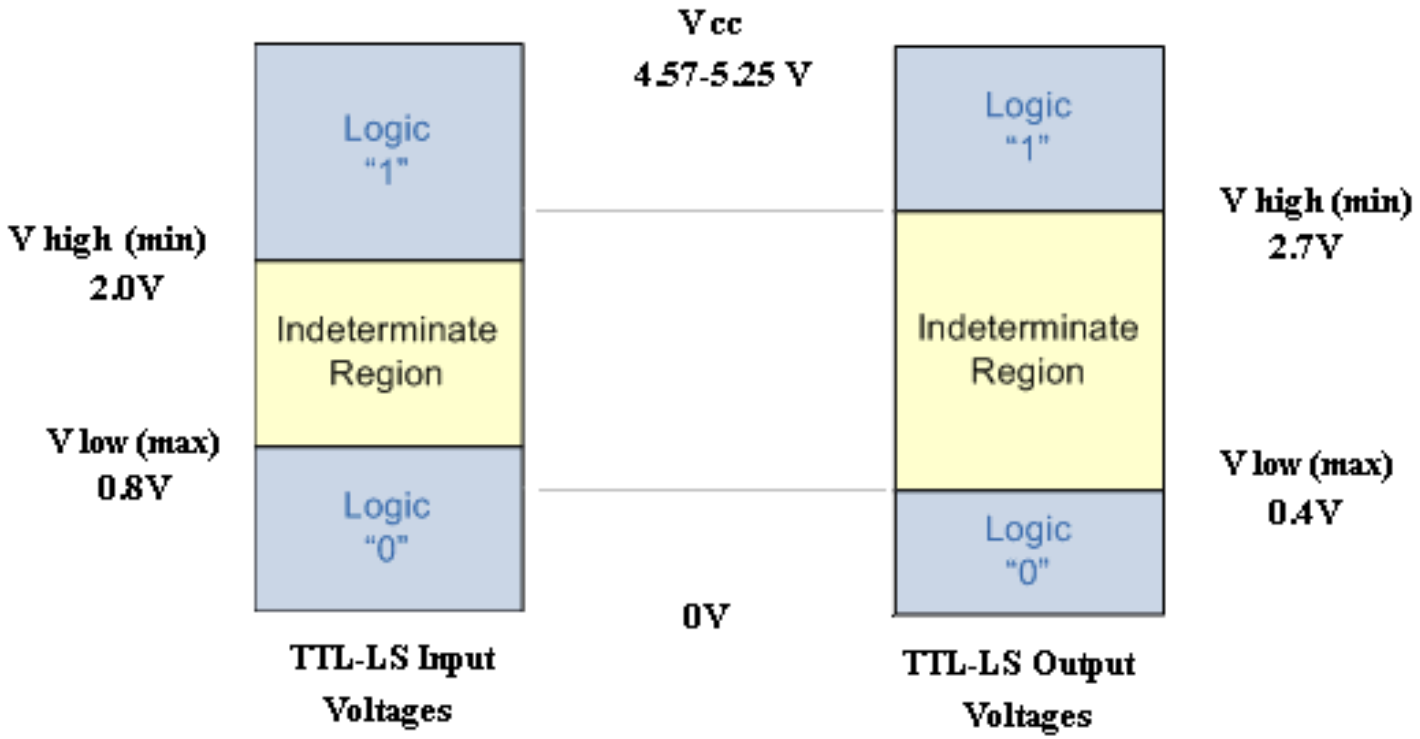
Logic Families Comparison

Family	Propagation delay (ns)	Power per gate @1 MHz (mW)	Typical supply voltage V	Notes
CMOS AC/ACT	3	0.5	3.3 or 5 (2-6 or 4.5 to 5.5)	ACT has TTL Compatible level
CMOS HC/HCT	9	0.5	5 (2-6)	HCT has TTL compatible levels
MOS 4000B/74C	30	1.2	10V (3-18)	
TTL	10	10	5 (4.75-5.25)	
TTL L	33	1	..	
TTL H	6	22	..	
TTL S	3	19	..	
TTL LS	10	2	..	
TTL ALS	4	1.3	..	
TTL F	3.5	5.4	..	
TTL AS	2	8	..	
ECL 100K	.75	40	-5.2(-4.9 - -5.5)	

Logic Families Voltage Levels



Input Output Standards

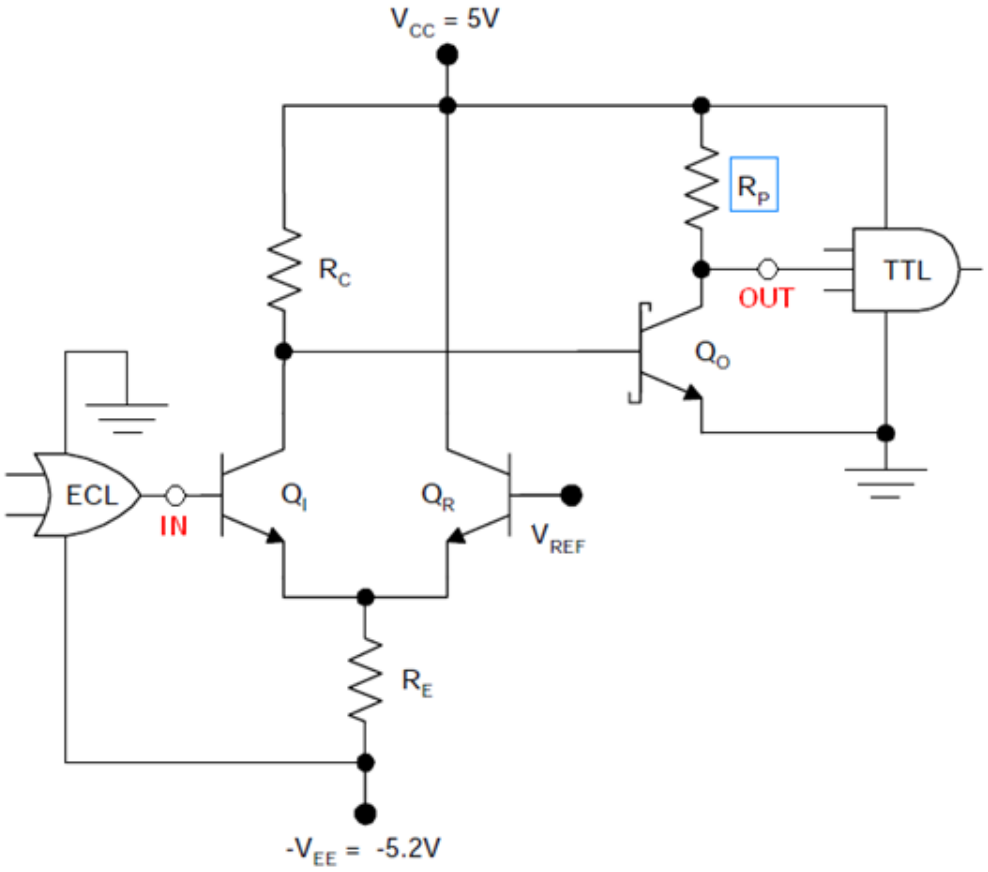


Logic Circuits Interfacing

Many applications require mixing logic families:

Different voltage levels → Level shifting circuits
→ Current driving

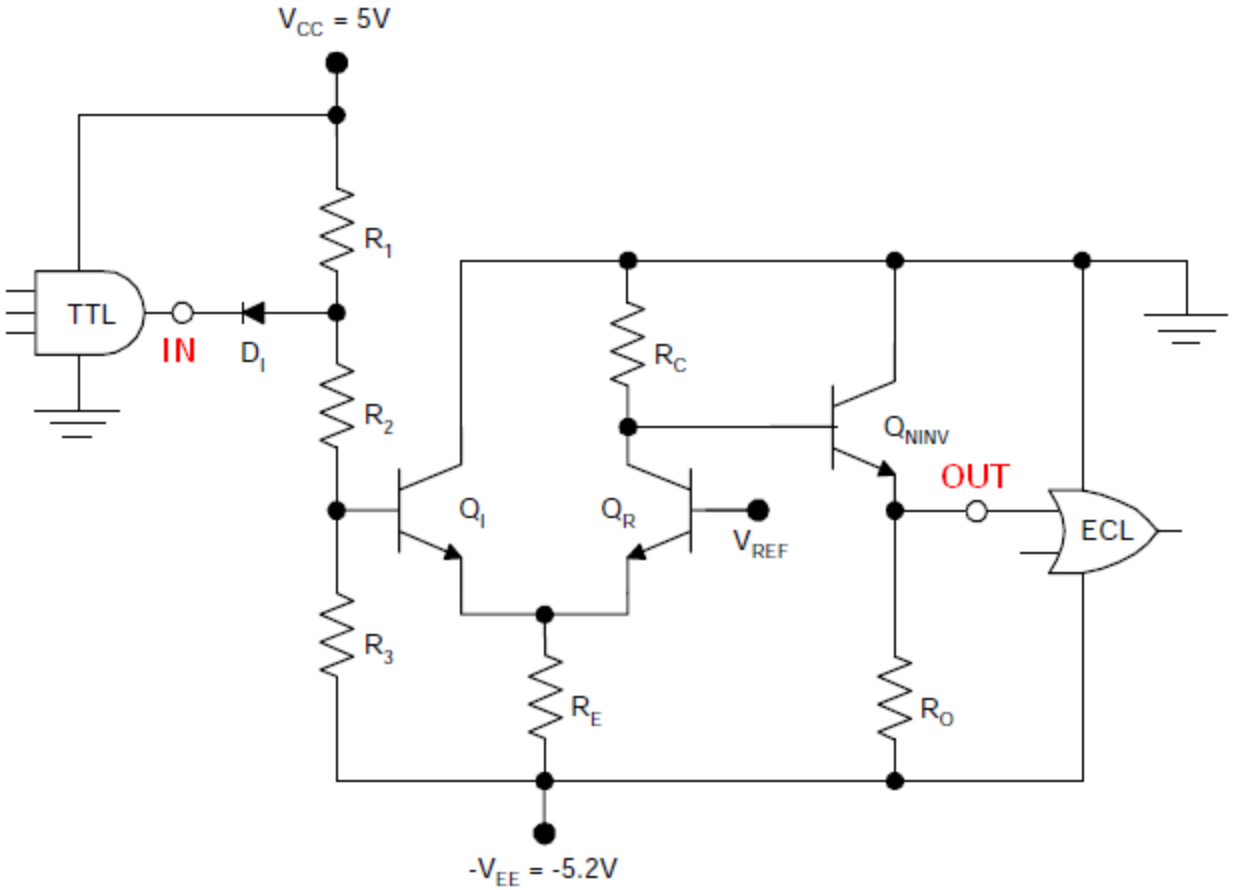
ECL to TTL



$V_{IN} = V_{OL}$ (ECL) $\rightarrow Q_I$ off $\rightarrow Q_O$ on hard$\rightarrow$ OUT$=V_{CE} = V_{OL}$(TTL)

$V_{IN} = V_{OH}$ (ECL) $\rightarrow Q_I$ on $\rightarrow Q_O$ off $\rightarrow$ OUT$= V_{DD} = V_{OH}$ (TTL)

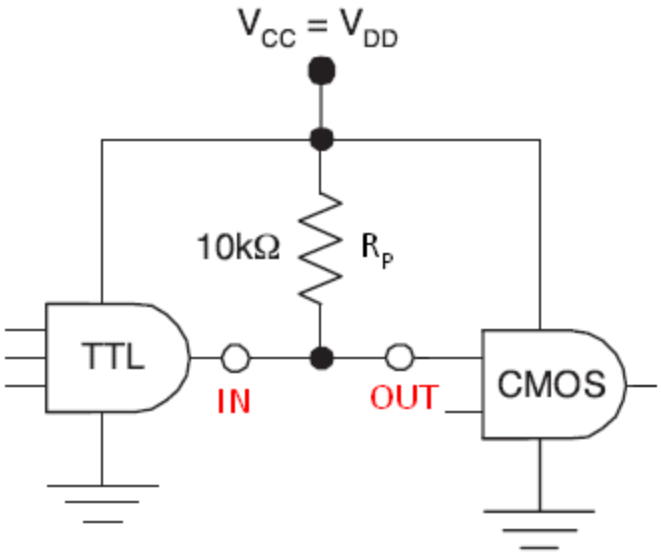
TTL to ECL



$$V_{IN} = V_{OL}\,(\text{TTL}) \rightarrow V_{BQI} < V_{REF} \rightarrow \text{Q}_\text{I}\ \text{off},\ \text{Q}_\text{R}\ \text{on} \rightarrow V_{OL}\,(\text{ECL})$$

$$V_{IN} = V_{OH}\,(\text{TTL}) \rightarrow \text{Q}_\text{I}\ \text{on},\ \text{Q}_\text{R}\ \text{off} \rightarrow V_{OH}\,(\text{ECL})$$

TTL to CMOS

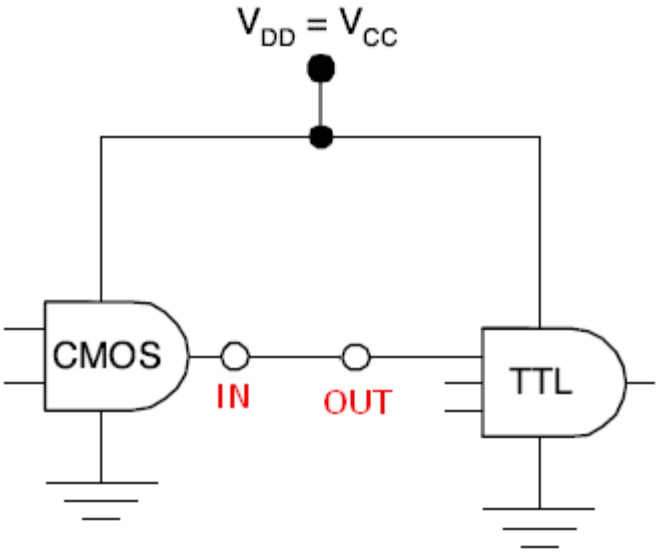


Simple because voltage levels are almost the same.

Pull-up resistor R_P forces OUT to V_{DD}.

Note: V_{OH} (TTL) < $V_{DD} - V_T$ (CMOS)

CMOS to TTL



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Thank You
&
Best Wishes

Omar Alasali